



PCI Graphics & Video Accelerator

PCI Graphics & Video Accelerator

SiS 6205

Preliminary

Rev. 2.0

March 21, 1996

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TABLE OF CONTENTS

| | |
|---|-----------|
| 1. Revision Notes..... | 1 |
| 2. SiS 6205 Overview | 1 |
| 2.1 Introduction..... | 1 |
| 2.2 Features..... | 2 |
| 2.3 Block Diagram..... | 5 |
| 2.3.1 SiS 6205/6204 System Block Diagram | 5 |
| 2.3.2 SiS 6205 VMI Interface Block Diagram | 7 |
| 2.3.3 SiS 6205 Block Diagram | 8 |
| 2.3.4 SiS 6205 Video Accelerator Block Diagram | 9 |
| 2.3.5 SiS 6205 and SiS 5511+, 5512, 5513 Shared Memory Architecture | 10 |
| 3. Function Description | 11 |
| 3.1 Functional Blocks | 11 |
| 3.1.1 Attribute Controller | 11 |
| 3.1.2 CRT Controller | 11 |
| 3.1.3 CRT FIFO..... | 11 |
| 3.1.4 DDC Controller..... | 11 |
| 3.1.5 Display Memory Controller | 11 |
| 3.1.6 DPMS | 11 |
| 3.1.7 Dual-Clock Synthesizer | 11 |
| 3.1.8 Graphics Controller | 11 |
| 3.1.9 Graphics Engine | 12 |
| 3.1.10 PCI Bus Interface | 15 |
| 3.1.11 RAMDAC..... | 15 |
| 3.1.12 Read-ahead Cache | 15 |
| 3.1.13 Video Accelerator | 15 |
| 3.1.14 Write FIFO..... | 16 |
| 3.2 BIOS ROM..... | 16 |
| 3.3 Bus Interface..... | 16 |
| 3.4 DRAM Support | 16 |
| 3.5 Video Memory Data Bus Architecture | 17 |
| 3.5.1 Memory Configuration Pins..... | 17 |
| 3.6 Internal Dual-Clock Synthesizer | 18 |
| 3.7 Power Management | 19 |
| 3.8 Resolutions Supported | 19 |
| 3.9 Turbo Queue..... | 19 |
| 3.10 Video Accelerator..... | 21 |



| | |
|---|-----------|
| 3.10.1 Video Password/Identification Register | 21 |
| 3.10.2 Video Play Back..... | 21 |
| 3.10.3 Feature Connector Interface | 21 |
| 3.10.4 Video Capture Window | 22 |
| 3.10.5 Video Captured Down Scaling..... | 22 |
| 3.10.6 Video Capture FIFO..... | 23 |
| 3.10.7 Multi-format Video Frame Buffer | 23 |
| 3.10.8 Video Playback Line Buffers..... | 23 |
| 3.10.9 Color Space Conversion & Color Format Conversion..... | 23 |
| 3.10.10 Horizontal Interpolation DDA | 23 |
| 3.10.11 Vertical Interpolation DDA | 24 |
| 3.10.12 Video Playback Horizontal Zooming | 24 |
| 3.10.13 Video Playback Vertical Zooming..... | 24 |
| 3.10.14 Video Data Blending | 24 |
| 3.10.15 Color Keying..... | 24 |
| 3.10.16 Chroma Keying..... | 24 |
| 3.10.17 Graphics & Video Overlay..... | 24 |
| 3.10.18 Video Window Control Registers | 25 |
| 3.10.19 Video Panning | 25 |
| 3.10.20 Overlay Memory Data | 26 |
| 3.11 Shared Memory | 26 |
| 3.12 Signature Analysis..... | 29 |
| 3.13 Compatibility | 30 |
| 3.14 Software Support..... | 30 |
| 4. Pin Description | 31 |
| 4.1 Pin Assignment | 31 |
| 4.1.1 Pin Outline | 31 |
| 4.1.2 Pin List..... | 32 |
| 4.2 Pin Definition..... | 36 |
| 4.2.1 PCI Bus Interface | 36 |
| 4.2.2 Display Memory Interface | 37 |
| 4.2.3 Clock Control..... | 38 |
| 4.2.4 Video/Video DAC Interface (In Standard FC mode)..... | 38 |
| 4.2.5 Video Input Interface (In Direct Video Mode & SiS FC mode)..... | 38 |
| 4.2.6 BIOS Interface | 39 |
| 4.2.7 DDC Interface..... | 39 |
| 4.2.8 Shared Memory Interface | 39 |
| 4.2.9 VMI Interface | 39 |
| 4.2.10 Misc. | 39 |
| 4.2.11 Power and Ground | 39 |



| | |
|--|-----------|
| 5. Mode Tables..... | 41 |
| 5.1 Standard VGA Modes..... | 41 |
| 5.2 Enhanced Video Modes | 43 |
| 6. Registers Description..... | 47 |
| 6.1 General Registers | 47 |
| 6.1.1 Miscellaneous Output Register | 47 |
| 6.1.2 Feature Control Register | 48 |
| 6.1.3 Input Status Register 0 | 48 |
| 6.1.4 Input Status Register 1 | 48 |
| 6.1.5 VGA Enable Register | 49 |
| 6.1.6 Segment Selection Register 0 | 49 |
| 6.1.7 Segment Selection Register 1 | 50 |
| 6.2 CRT Controller Registers..... | 51 |
| 6.2.1 CRT Controller Index Register..... | 51 |
| 6.2.2 CR0: Horizontal Total..... | 52 |
| 6.2.3 CR1: Horizontal Display Enable End..... | 52 |
| 6.2.4 CR2: Horizontal Blank Start..... | 52 |
| 6.2.5 CR3: Horizontal Blank End | 52 |
| 6.2.6 CR4: Horizontal Retrace Start..... | 52 |
| 6.2.7 CR5: Horizontal Retrace End | 52 |
| 6.2.8 CR6: Vertical Total | 53 |
| 6.2.9 CR7: Overflow Register | 53 |
| 6.2.10 CR8: Preset Row Scan | 53 |
| 6.2.11 CR9: Maximum Scan Line/Text Character Height | 53 |
| 6.2.12 CRA: Text Cursor Start..... | 53 |
| 6.2.13 CRB: Text Cursor End | 54 |
| 6.2.14 CRC: Screen Start Address High..... | 54 |
| 6.2.15 CRD: Screen Start Address Low | 54 |
| 6.2.16 CRE: Text Cursor Location High | 54 |
| 6.2.17 CRF: Text Cursor Location Low | 54 |
| 6.2.18 CR10: Vertical Retrace Start | 54 |
| 6.2.19 CR11: Vertical Retrace End | 55 |
| 6.2.20 CR12: Vertical Display Enable End | 55 |
| 6.2.21 CR13: Screen Offset..... | 55 |
| 6.2.22 CR14: Underline Location Register | 55 |
| 6.2.23 CR15: Vertical Blank Start | 56 |
| 6.2.24 CR16: Vertical Blank End | 56 |
| 6.2.25 CR17: Mode Control Register | 56 |
| 6.2.26 CR18: Line Compare Register | 56 |
| 6.2.27 CR19: Extended Signature Read-Back Register 0..... | 57 |
| 6.2.28 CR1A: Extended Signature Read-Back Register 1 | 57 |



6.2.29 CR22: Graphics Data Latch Readback Register 57

6.2.30 CR24: Attribute Controller Toggle Readback Register 57

6.2.31 CR26: Attribute Controller Index Readback Register 57

6.3 Sequencer Registers 58

6.3.1 Sequencer Index Register 58

6.3.2 SR0: Reset Register 58

6.3.3 SR1: Clock Mode Register 58

6.3.4 SR2: Color Plane Write Enable Register 59

6.3.5 SR3: Character Generator Select Register 59

6.3.6 SR4: Memory Mode Register 60

6.4 Graphics Controller Registers 61

6.4.1 Graphics Controller Index Register 61

6.4.2 GR0: Set/Reset Register 61

6.4.3 GR1: Set/Reset Enable Register 61

6.4.4 GR2: Color Compare Register 62

6.4.5 GR3: Data Rotate/Function Select Register 62

6.4.6 GR4: Read Plane Select Register 62

6.4.7 GR5: Mode Register 63

6.4.8 GR6: Miscellaneous Register 64

6.4.9 GR7: Color Don't Care Register 64

6.4.10 GR8: Bit Mask Register 64

6.5 Attribute Controller and Video DAC Registers 65

6.5.1 Attribute Controller Index Register 65

6.5.2 AR0~ARF: Palette Registers 66

6.5.3 AR10: Mode Control Register 66

6.5.4 AR11: Screen Border Color 67

6.5.5 AR12: Color Plane Enable Register 67

6.5.6 AR13: Pixel Panning Register 67

6.5.7 AR14: Color Select Register 68

6.6 Color Registers 69

6.6.1 DAC Status Register 69

6.6.2 DAC Index Register (Read Mode) 69

6.6.3 DAC Index Register (Write Mode) 69

6.6.4 DAC Data Register 69

6.6.5 PEL Mask Register 69

6.7 SiS 6205 Extended Registers 70

6.7.1 Extended Index Register 70

6.7.2 SR5: Extended Password/Identification Register 71

6.7.3 SR6: Extended Graphics Mode Control Register 71

6.7.4 SR7: Extended Misc. Control Register 0 72

6.7.5 SR8: Extended CRT/CPU Threshold Control Register 0 72



| | |
|--|----|
| 6.7.6 SR9: Extended CRT/CPU Threshold Control Register 1..... | 72 |
| 6.7.7 SRA: Extended CRT Overflow Register..... | 72 |
| 6.7.8 SRB: Extended Misc. Control Register 1..... | 73 |
| 6.7.9 SRC: Extended Misc. Control Register 2..... | 73 |
| 6.7.10 SRD: Extended Configuration Status 0..... | 74 |
| 6.7.11 SRE: Extended Configuration Status 1..... | 74 |
| 6.7.12 SRF: Extended Scratch Register 0..... | 75 |
| 6.7.13 SR10: Extended Scratch Register 1..... | 75 |
| 6.7.14 SR11: Extended DDC and Power Control Register..... | 75 |
| 6.7.15 SR14: Extended Hardware Cursor Color 0 Red Register..... | 76 |
| 6.7.16 SR15: Extended Hardware Cursor Color 0 Green Register..... | 76 |
| 6.7.17 SR16: Extended Hardware Cursor Color 0 Blue Register..... | 76 |
| 6.7.18 SR17: Extended Hardware Cursor Color 1 Red Register..... | 76 |
| 6.7.19 SR18: Extended Hardware Cursor Color 1 Green Register..... | 76 |
| 6.7.20 SR19: Extended Hardware Cursor Color 1 Blue Register..... | 76 |
| 6.7.21 SR1A: Extended Hardware Cursor Horizontal Start Register 0..... | 77 |
| 6.7.22 SR1B: Extended Hardware Cursor Horizontal Start Register 1..... | 77 |
| 6.7.23 SR1C: Extended Hardware Cursor Horizontal Preset Register..... | 77 |
| 6.7.24 SR1D: Extended Hardware Cursor Vertical Start Register 0..... | 77 |
| 6.7.25 SR1E: Extended Hardware Cursor Vertical Start Register 1..... | 77 |
| 6.7.26 SR1F: Extended Hardware Cursor Vertical Preset Register..... | 77 |
| 6.7.27 SR20: Extended Linear Addressing Base Address Register 0..... | 78 |
| 6.7.28 SR21: Extended Linear Addressing Base Address Register 1..... | 78 |
| 6.7.29 SR22: Extended Standby/Suspend Timer Register..... | 78 |
| 6.7.30 SR23: Extended Misc. Control Register 3..... | 78 |
| 6.7.31 SR24: Extended Graphics Frame Buffer Location Address Register..... | 79 |
| 6.7.32 SR25: Extended Scratch Register 2..... | 79 |
| 6.7.33 SR26: Extended Graphics Engine Register 0..... | 79 |
| 6.7.34 SR27: Extended Graphics Engine Register 1..... | 80 |
| 6.7.35 SR28: Extended Internal Memory Clock Register 0..... | 80 |
| 6.7.36 SR29: Extended Internal Memory Clock Register 1..... | 80 |
| 6.7.37 SR2A: Extended Internal Video Clock Register 0..... | 81 |
| 6.7.38 SR2B: Extended Internal Video Clock Register 1..... | 81 |
| 6.7.39 SR2C: Extended Turbo Queue Base Address..... | 81 |
| 6.7.40 SR2D: Extended Memory Start Control Register..... | 81 |
| 6.7.41 SR2E: Extended Shared Memory Control Register..... | 82 |
| 6.7.42 SR2F: Extended DRAM Frame Buffer Size Register..... | 82 |
| 6.7.43 SR30: Extended Reserved Register..... | 83 |
| 6.7.44 SR31: Extended Reserved Register..... | 83 |
| 6.7.45 SR32: Extended Reserved Register..... | 83 |
| 6.7.46 SR33: Extended Reserved Register..... | 84 |
| 6.7.47 SR34: Extended Reserved Register..... | 84 |



| | |
|--|-----|
| 6.7.48 SR35: Extended Reserved Register..... | 84 |
| 6.7.49 SR36: Extended Scratch Register 3 | 84 |
| 6.7.50 SR37: Extended Scratch Register 4 | 84 |
| 6.8 Graphics Engine Related Registers | 85 |
| 6.8.1 Register Format for General Engine Functions | 85 |
| 6.8.2 Register Format for Line Drawing | 90 |
| 6.8.3 The Register Format for Direct Draw | 94 |
| 6.9 Video Accelerator Registers..... | 99 |
| 6.9.1 Password/Identification Register..... | 100 |
| 6.9.2 Video Window Horizontal Display Start Low Register | 100 |
| 6.9.3 Video Window Horizontal Display End Low Register | 100 |
| 6.9.4 Video Window Horizontal Display Overflow Register | 100 |
| 6.9.5 Video Window Vertical Display Start Low Register | 101 |
| 6.9.6 Video Window Vertical Display End Low Register..... | 101 |
| 6.9.7 Video Window Vertical Display Overflow Register | 101 |
| 6.9.8 Video Capture Frame Buffer Starting Address Low Register | 101 |
| 6.9.9 Video Capture Frame Buffer Starting Address Middle Register | 102 |
| 6.9.10 Video Frame Buffer Overflow Register..... | 102 |
| 6.9.11 Video Display Frame Buffer Starting Address Low Register | 102 |
| 6.9.12 Video Display Frame Buffer Starting Address Middle Register | 102 |
| 6.9.13 Video Frame Buffer Offset Low Register..... | 102 |
| 6.9.14 Video Display Frame Buffer End Address Low Register | 103 |
| 6.9.15 Video Frame Buffer Offset Address High Register | 103 |
| 6.9.16 Video Capture Threshold Value Register..... | 103 |
| 6.9.17 Video Capture Horizontal Down Scaling Factor Register..... | 103 |
| 6.9.18 Video Capture Vertical Down Scaling Register..... | 104 |
| 6.9.19 Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register..... | 104 |
| 6.9.20 Vertical Up Scaling Factor Register..... | 104 |
| 6.9.21 Horizontal Scaling Factor Integer Register..... | 105 |
| 6.9.22 Video Overlay Color Key Blue Low Value Register | 105 |
| 6.9.23 Video Overlay Color Green Low Value Register | 105 |
| 6.9.24 Video Overlay Color Red Low Value Register..... | 106 |
| 6.9.25 Video Control Misc. Register 0 | 106 |
| 6.9.26 Video Control Misc. Register 1 | 107 |
| 6.9.27 Video Chroma Key B/Y Low Value Register..... | 107 |
| 6.9.28 Video Chroma Key G/U Low Value Register | 108 |
| 6.9.29 Video Chroma Key R/V Low Value Register..... | 108 |
| 6.9.30 Video Control Misc. Register 3 | 108 |
| 6.9.31 Video Playback Threshold Low Value Register | 109 |
| 6.9.32 Video Playback Threshold High Value Register | 109 |



| | |
|--|------------|
| 6.9.33 Line Buffer Size Register | 110 |
| 6.9.34 Video Overlay Color Key Blue High Value Register | 110 |
| 6.9.35 Video Overlay Color Key Green High Value Register | 110 |
| 6.9.36 Video Overlay Color Key Red High Value Register | 110 |
| 6.9.37 Video Chroma Key B/Y High Value Register | 111 |
| 6.9.38 Video Chroma Key G/U High Value Register | 111 |
| 6.9.39 Video Chroma Key R/V High Value Register | 111 |
| 6.9.40 Graphics Data Alpha Value Register | 112 |
| 6.9.41 Video Data Alpha Value Register | 112 |
| 6.9.42 Key Overlay Operation Mode Register | 112 |
| 6.9.43 Video Capture Horizontal Start Register..... | 113 |
| 6.9.44 Video Capture Horizontal End Register | 113 |
| 6.9.45 Video Capture Vertical Start Register..... | 114 |
| 6.9.46 Video Capture Vertical End Register | 114 |
| 6.9.47 Video Capture Horizontal Overflow Register..... | 115 |
| 6.9.48 Video Capture Vertical Overflow Register..... | 115 |
| 6.9.49 System Memory Video Frame Buffer Setting Register 1 | 115 |
| 6.9.50 System Memory Video Frame Buffer Setting Register 2 | 116 |
| 6.9.51 System Memory Video Frame Buffer Setting Reg. 3 and Video Control Reg. .. | 116 |
| 6.10 PCI Configuration Registers..... | 117 |
| 6.10.1 Configuration Register 00h..... | 117 |
| 6.10.2 Configuration Register 04h..... | 117 |
| 6.10.3 Configuration Register 08h..... | 117 |
| 6.10.4 Configuration Register 10h..... | 117 |
| 6.10.5 Configuration Register 14h..... | 117 |
| 6.10.6 Configuration Register 18h..... | 118 |
| 6.10.7 Configuration Register 2Ch | 118 |
| 6.10.8 Configuration Register 30h..... | 118 |
| 6.10.9 Configuration Register 3Ch | 118 |
| 7. Electrical Characteristics..... | 119 |
| 7.1 Absolute Maximum Ratings..... | 119 |
| 7.2 DC Characteristics..... | 119 |
| 7.3 DC Characteristics for DAC (Analog Output Characteristics) | 119 |
| 7.4 AC Characteristics for DAC (Analog Output Characteristics) | 119 |
| 7.5 AC Characteristics..... | 120 |
| 8. Mechanical Dimension | 129 |
| 9. Appendix A. Recommended Memory Configuration..... | 130 |
| 10. Appendix B. Product Change Notice For Rev. Dx | 134 |
| 11. COPYRIGHT NOTICE | 136 |





1. Revision Notes

This document describes the SiS 6205 Rev. Dx detail technical information. All the information contained in this document can only be applied to SiS 6205 Rev. Dx chips. For the previous version SiS 6205, please refer to their own data sheet for correct information.

In Appendix B, we highlight the major differences between Rev. Dx and previous version. For those who may concern this issue, please refer to Appendix B on page 134.

2. SiS 6205 Overview

2.1 Introduction

To provide a compact video and graphics solution for PC based system, SiS has created a new counter parts SiS 6204 and 6205 to fit the market demand.

SiS 6204 is a video interface chip which lies on ISA bus and interface to both PC-Video decoder and/or MPEG decoder. The video data would be transferred from MPEG decoder and/or PC-Video decoder to SiS 6204. After receiving these original video data, SiS 6204 would perform YUV-to-RGB conversion, filter, dithering, and transfer the modified video data through SiS proprietary defined feature connector to SiS 6205 for further handling.

SiS 6205 is a high performance 3-in-1 PCI true-color graphics accelerator with video accelerate functions. SiS 6205 video accelerator could work in five different modes: standard FC (Feature Connector) mode, SiS FC (SiS Proprietary Defined Feature Connector) mode, direct video mode, VMI (Video Module Interface) interface mode, and PCI multimedia mode.

Furthermore SiS 6205 could work with SW MPEG Player Programs through DCI driver or Direct Draw driver to provide high performance SW MPEG playback to meet future PC trends.

In SiS FC mode, after receiving the video data from SiS 6204, SiS 6205 would perform scaling and store these scaled video data to the display memory. Furthermore SiS 6205 would perform color-space conversion, interpolation, and scaling on the stored video data before overlaying with graphics data for final display.

In direct video mode, SiS 6205 could work with the Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2), to provide the PC-Video solution and provide the very flexible overlaying ability mentioned above.

In VMI interface mode, SiS 6205 partially supports VMI interface spec (Some VMI signals must come from ISA bus, therefore suit for all-in-one mother board design.) to connect to other devices support the VMI spec.

In PCI multimedia mode, SiS 6205 supports PCI multimedia design guide Rev. 1.0 spec to meet future potential trend.

SiS 6205 also supports shared memory architecture to share main board memory with SiS 5511+/5512/5513 chipset or other main board chipsets support the same architecture.



2.2 Features

PCI Bus Interface

- Supports 32-bit PCI local bus standard Revision 2.1
- Supports PCI burst write
- Supports PCI multi-function device
- Follows the one-load-per-slot PCI specification
- Supports PCI multimedia design guide Rev. 1.0

Performance

- Supports Turbo Queue (Software Command Queue in off-screen memory) architecture to achieve extra-high performance (patent pending)
- Built-in Direct Draw Accelerator
- Built-in an enhanced 64-bit BITBLT graphics engine with the following functions:
 - 256 raster operation functions
 - Rectangle fill
 - Color/Font expansion
 - Enhanced Color expansion
 - Enhanced Font expansion
 - Line-drawing with styled pattern
 - Built-in 8x8 pattern registers
 - Built-in 8x8 mask registers
 - 32 doublewords Command Queue
- Built-in 64x64x2 bit-mapped hardware cursor
- Built-in 6 stages CPU write-buffer and 128 bits read-ahead cache to minimize CPU wait-state
- Built-in 2 stages engine write-buffer and 320 bits read-buffer to minimize engine wait-state
- Built-in 64x32 CRT FIFOs to support super high resolution graphics modes and reduce CPU wait-state
- Memory-mapped I/O to reduce I/O trapping overhead under protected mode
- Supports linear addressing mode up to 4MByte to speed up graphics performance
- Supports shared memory for both system memory and display memory

Integration

- Built-in programmable 24-bit true-color RAMDAC with reference-voltage generator
- Built-in dual-clock generator
- Built-in monitor-sense circuit
- Built-in graphics accelerator and VGA controller
- Built-in video accelerator
- Built-in Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) video decoder interface
- Built-in SiS proprietary defined 8-bit feature connector logic for direct connecting to SiS 6204 for video overlay



- Partially supports VMI (Video Module Interface) to connect to VMI device
- Built-in standard feature connector logic support
- Built-in PCI multimedia interface

Display Memory Interface

- 64-bit display memory data bus architecture with up to 240 MByte/sec peak memory bandwidth by using 2 banks or 4 banks of DRAM.
- Supports 256Kx4, 256Kx8, and 256Kx16 DRAM and EDO DRAM types
- Supports 2-CAS/1-WE and 2-WE/1-CAS 256Kx16 DRAM and EDO DRAM types
- Supports 32/64-bit display memory path
- Supports 1MB, 2MB, and 4MB DRAM configuration at non-shared memory architecture
- Supports 0.5MB, 1MB, 1.5MB, 2MB, 2.5MB, 3MB, 3.5MB, and 4MB DRAM configuration at shared-memory architecture
- Supports auto memory size detecting

Resolution, Color & Frame Rate

- Supports 135 MHz pixel clock
- Supports super high resolution graphics modes
 - 640x480 256/32K/64K/16M colors NI
 - 800x600 16/256/32K/64K/16M colors NI
 - 1024x768 16/256/32K/64K/16M colors NI
 - 1280x1024 16/256 colors NI, 32k/64k colors interlace only
- Supports virtual screen up to 2048x2048
- Supports 80/132 columns text mode in 25, 30, 44, or 60 rows and other modes
- Supports 85Hz vertical refresh rate

Video Functions

- Supports full motion picture required only 1 Megabyte DRAM and up to 1024x768x256-color mode
- Built-in Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) video decoder interface
- Built-in SiS proprietary defined 8-bit feature connector logic for direct connecting to SiS 6204 for video overlay
- Partially supports VMI (Video Module Interface) interface to connect to other VMI devices
- Built-in standard feature connector logic support
- Built-in PCI multimedia interface
- Supports single frame buffer architecture to save the DRAM cost
- Supports graphics/video overlay function by color-key and/or chroma-key operation
- Supports multi-format Video For Windows such as YUV411, YUV422, RGB565, and RGB555
- Supports YUV-to-RGB color space conversion
- Supports video scaling in integer increments of 1/64



- Supports horizontal 2-tap, 8-phase DDA interpolation
- Supports vertical 2-tap, 8-phase DDA interpolation for better quality of video windows expansion
- Built-in 64x16 video capture FIFOs to support video capture
- Built-in two 64x90 video playback line buffers to support video playback
- Supports Microsoft Video For Windows
- Supports color key and chroma key overlay
- Supports 3-bit blending
- Supports DCI Drivers
- Supports Direct Draw Drivers

Power Management

- Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management
- Built-in 30 min. standby and suspend timers with keyboard, hardware cursor, and/or video memory read/write as activation source
- Supports direct I/O command to force graphics controller into standby/suspend/off state
- Power down internal SRAM in direct color mode
- Built-in a low power signal pin for supporting external power down controller

Multimedia Application

- Supports DDC1 and DDC2B specifications
- Follows the plug & play specification for display controller
- Supports RAMDAC snoop for multimedia applications

Misc.

- Only 4 ICs (including DRAMs) required to implement a PCI true-color graphics adapter without any TTLs
- Supports Signature Analysis for automatic test
- Supports 64KBytes ROM decoding
- Implemented by sub-micron CMOS technology in 208-pin PQFP package

2.3 Block Diagram

2.3.1 SiS 6205/6204 System Block Diagram

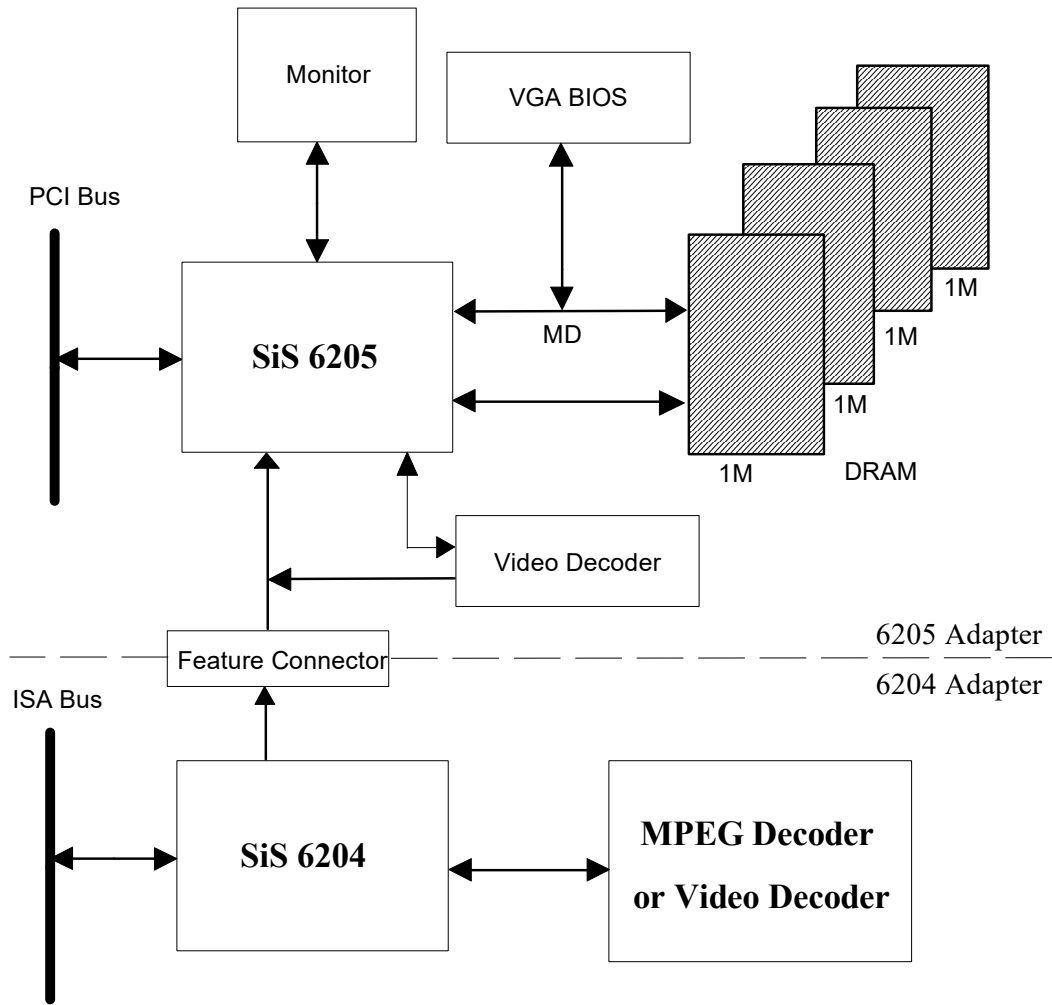


Figure 2.1

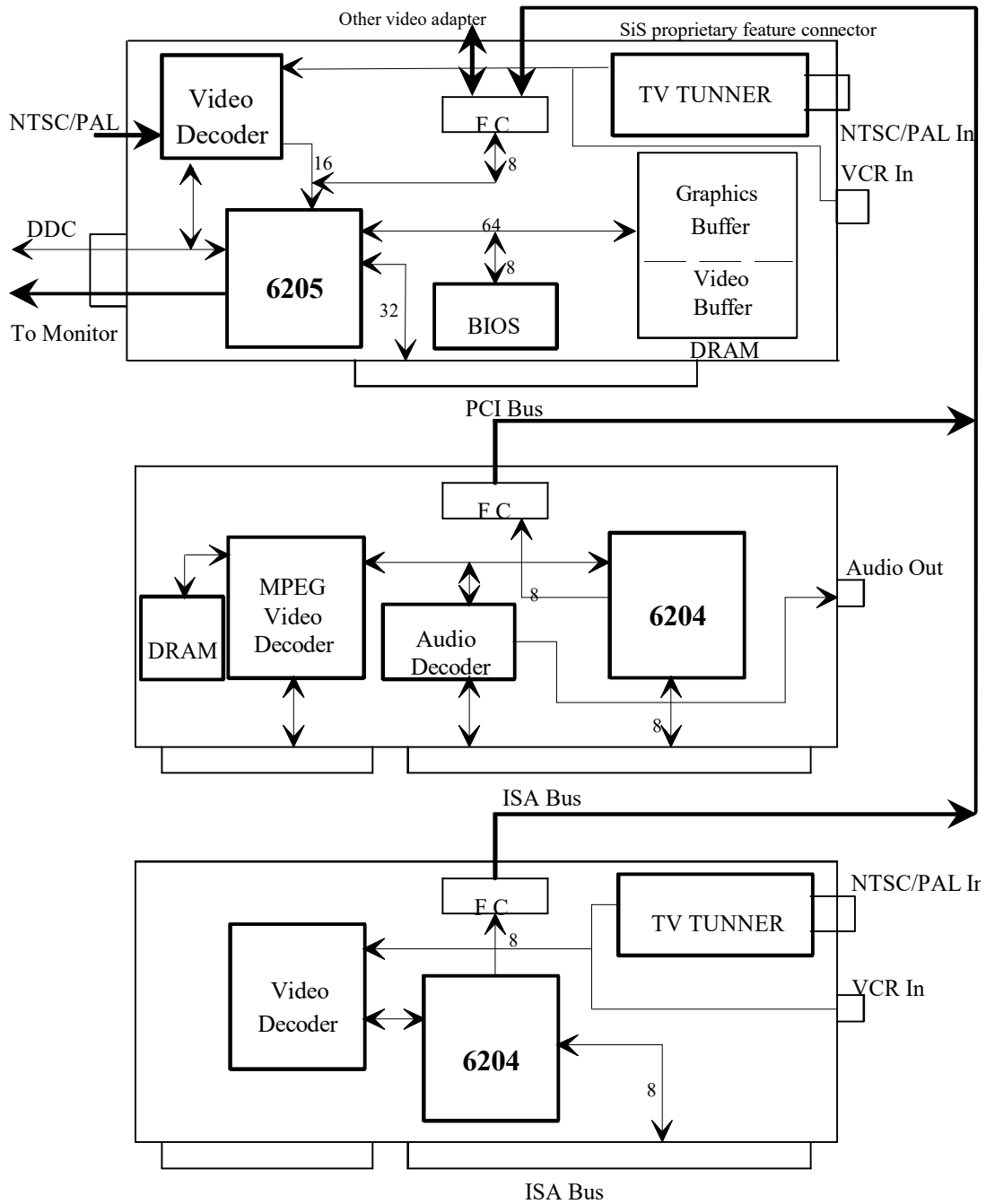


Figure 2.2

2.3.2 SiS 6205 VMI Interface Block Diagram

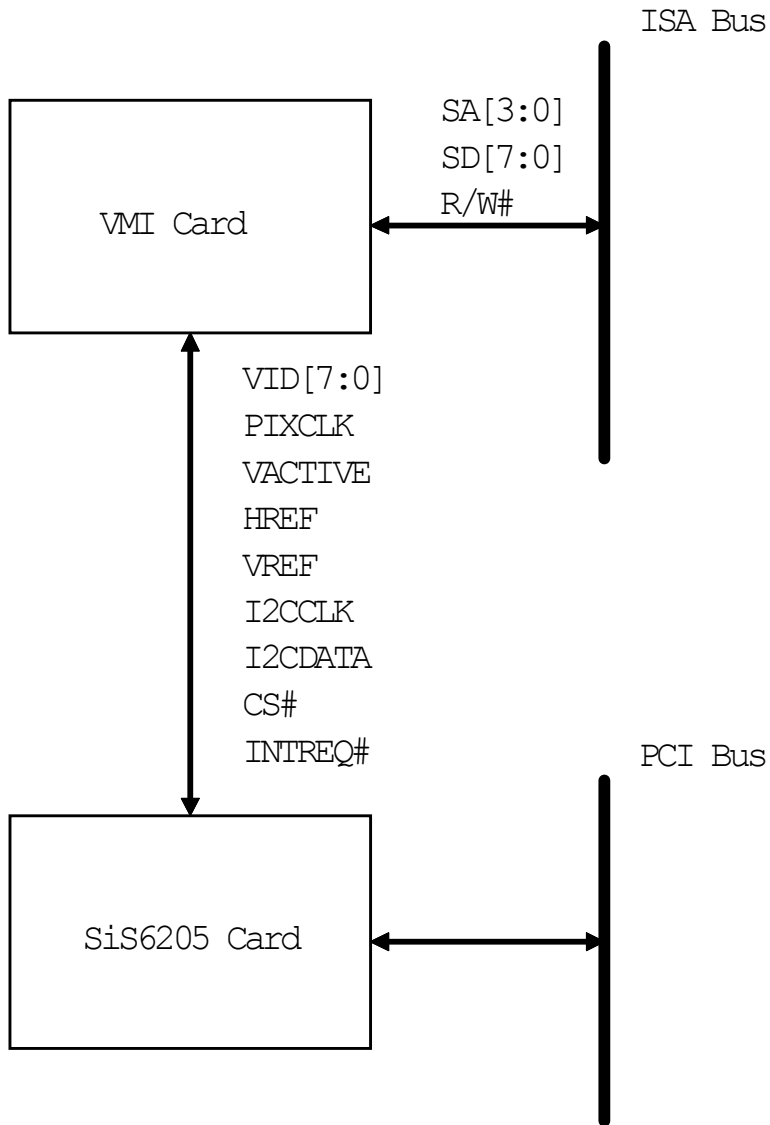


Figure 2.3

2.3.3 SiS 6205 Block Diagram

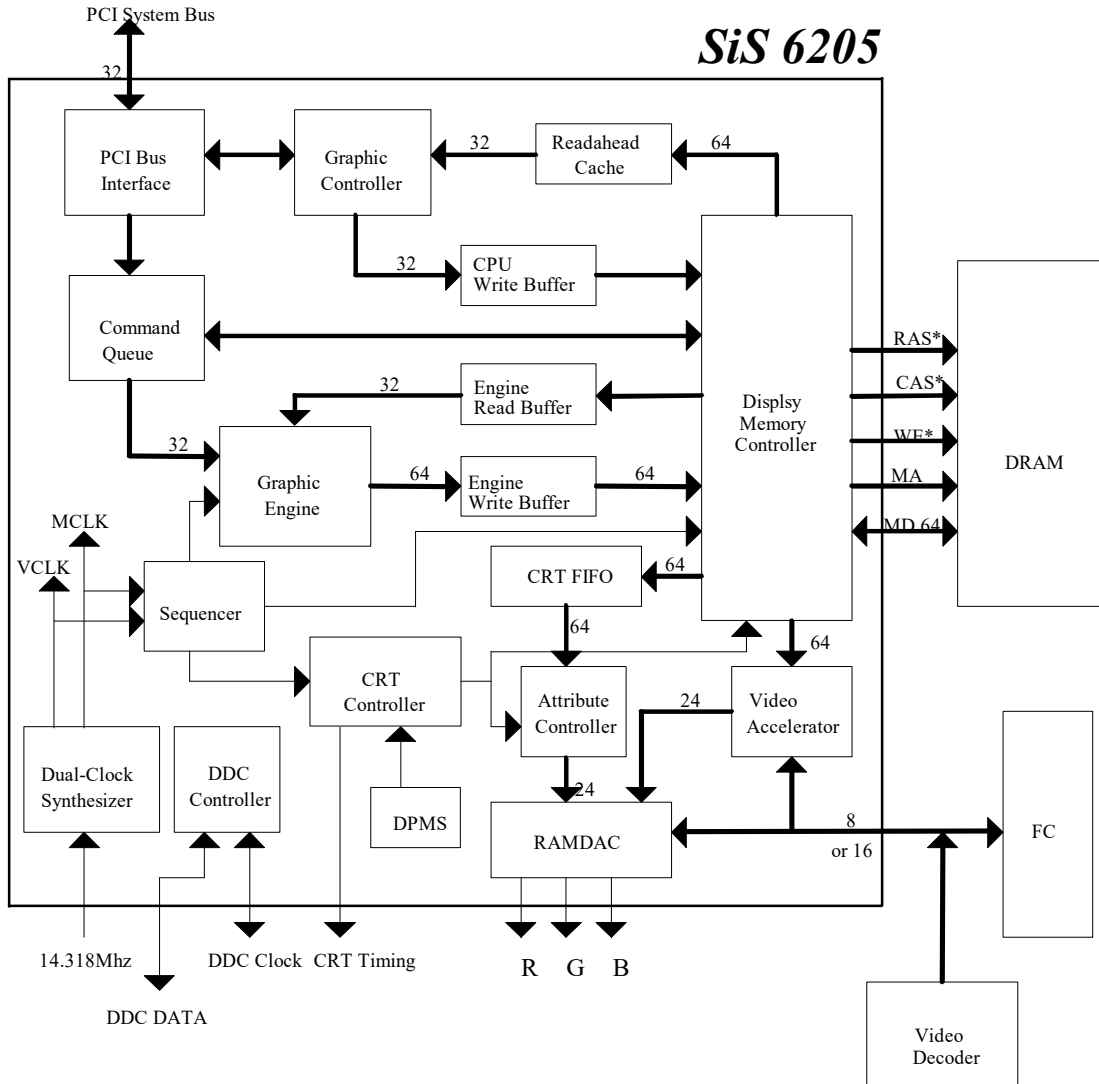


Figure 2.4

2.3.4 SiS 6205 Video Accelerator Block Diagram

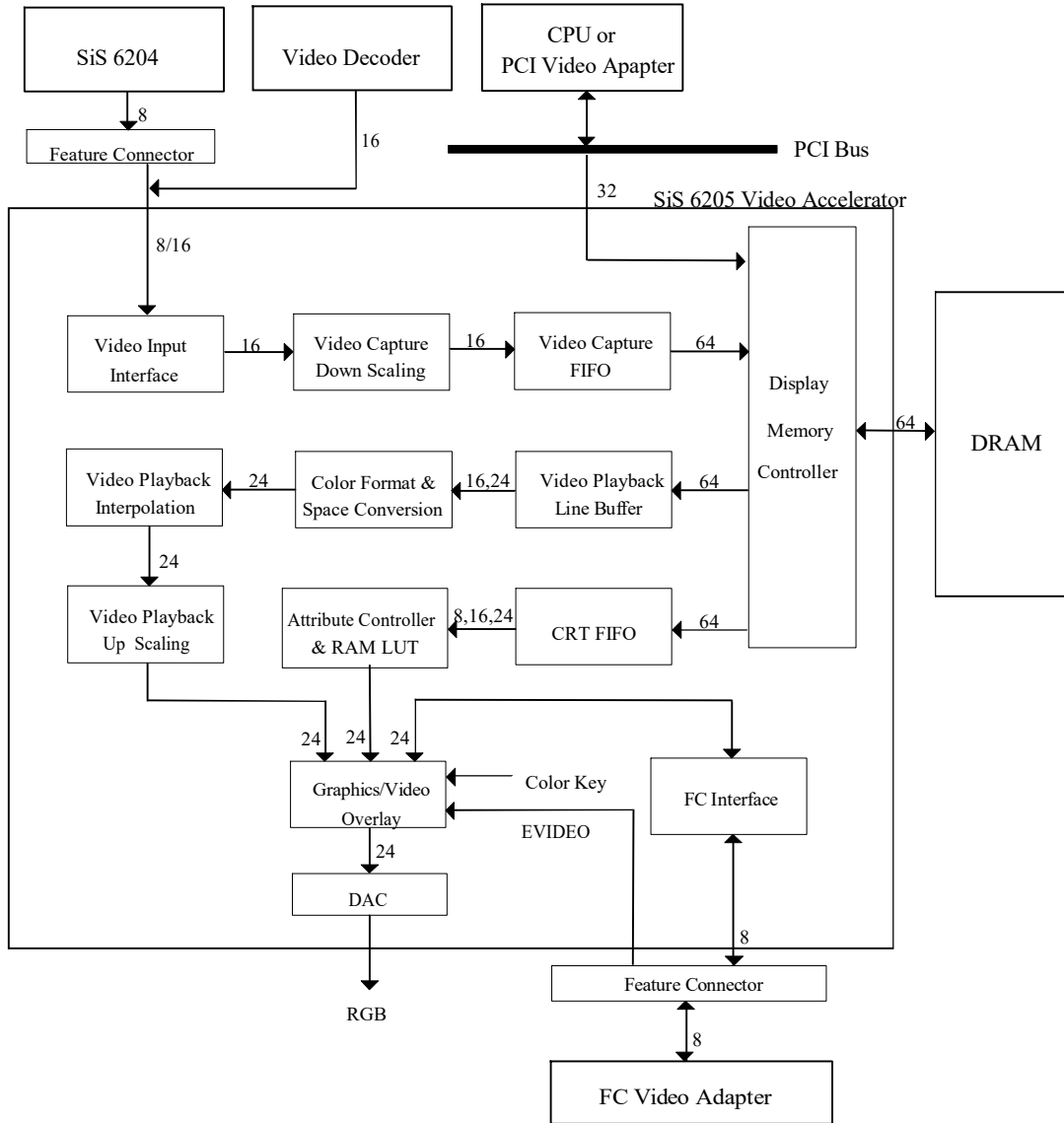


Figure 2.5

2.3.5 SiS 6205 and SiS 5511+, 5512, 5513 Shared Memory Architecture

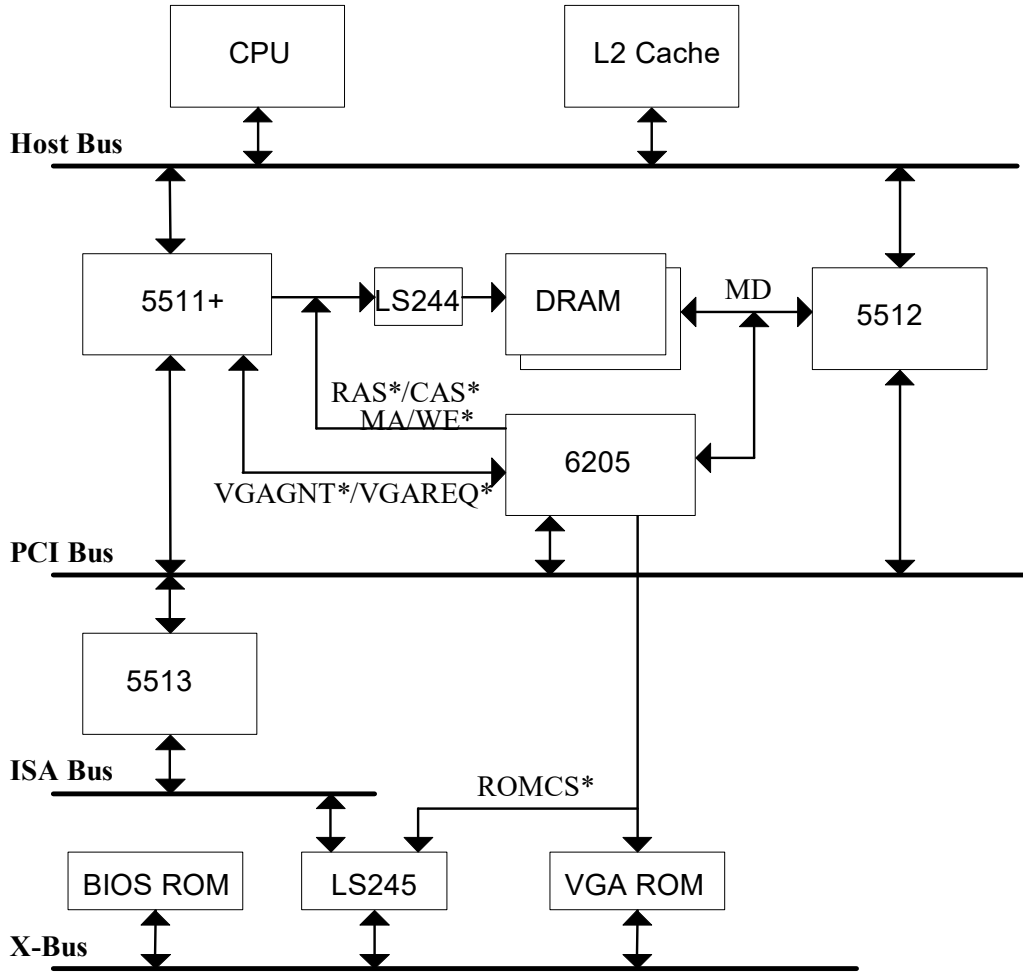


Figure 2.6



3. Function Description

3.1 Functional Blocks

3.1.1 Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking, alternate font selection, and underlining are performed by the Attribute Controller.

3.1.2 CRT Controller

The CRT Controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the Attribute Controller.

3.1.3 CRT FIFO

The 64x32 CRT FIFO allows the Display Memory Controller to access the display memory for screen refresh at maximum memory speed rather than at the screen refresh rate. It provides 3 programmable thresholds - CRT/CPU Threshold Low, CRT/CPU Threshold High, and CRT/Engine Threshold High. With adequate programming these three thresholds, the CPU wait-time would be reduced to improve the graphics performance.

3.1.4 DDC Controller

The DDC Controller provides two different channels to communicate with the monitor which supports DDC level 1 or DDC level 2B. One is DDC CLK channel which is bidirectional and provides the clock for DDC. The other is DDC DATA channel which is bidirectional and could query some information from monitor.

With the advantage of DDC, VGA BIOS could realize the capability of the connected monitor and take adequate action (such as to program the parameters for higher frame rate, ..., etc.) to make end users feel more comfortable.

3.1.5 Display Memory Controller

The Display Memory Controller generates timing for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE*.

3.1.6 DPMS

It provides some registers to control the CRT timing to be compatible with the VESA DPMS specification. (For detail description, refer to "3.7 Power Management".)

3.1.7 Dual-Clock Synthesizer

The Dual-Clock Synthesizer generates MCLK and VCLK with single external reference clock. With this character, we could set the MCLK at the maximum speed which the display memory could work normally, thus it takes the advantage of the real peak memory bandwidth and improves the graphics performance. (For detail description, refer to "3.6 Internal Dual-Clock Synthesizer".)

3.1.8 Graphics Controller

It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

3.1.9 Graphics Engine

It is an enhanced 64-bit BitBlt Graphics Engine.

For enhanced 256-color graphics mode, the engine supports the following functions:

- 256 Raster Operation Functions
- Rectangle Fill
- Color/Font Expansion
- Enhanced Color expansion
- Enhanced Font expansion
- Line Drawing
- Built-in 8x8 Pattern Registers
- Built-in 8x8 Mask Registers
- Direct Draw

For 32K or 64K high-color graphics mode, the engine supports the following functions:

- 256 Raster Operation Functions
- Rectangle Fill
- Color/Font Expansion
- Enhanced Color expansion
- Enhanced Font expansion
- Line Drawing
- Built-in 8x8 Mask Registers
- Direct Draw

For 16M-color graphics mode, due to different graphics process methods, the engine supports the following functions:

- Source/Destination BitBlt
- Pattern/Destination BitBlt
- Color/Font Expansion
- Enhanced Font expansion

Descriptions of the graphics engine functions are summarized as follows:

Bit Block Transfer (BitBlt)

BitBlt moves a block of data from one location (source) to another location (destination). It is a ternary operation. The operands could be the source data, the destination data, and the brush pattern. There are three different kinds of BitBlt: from the host memory to the display memory, from the display memory to the host memory, and from one location of the display memory to another location of the display memory.

In the first two cases, the operation simply uses the "move string instruction" (REP MOVS) to move the source data to the destination to accomplish the BitBlt operation. It is called "CPU-driven BitBlt".

In the case of moving from the display memory to the display memory, integrated Graphics Controller could gain the advantage of its advanced engine design to solve the problems of memory overlapping during the block transfers. The only effort is to program the adequate parameters.



BitBlt with Mask

When the BitBlt operation deals with the hatched brush pattern, the programmer just needs to set the monochrome mask into Mask Registers and program an adequate BG Rop and Background Color, then the engine would handle the complicated process.

Color/Font Expansion

The color/font expansion is used to expand a monochrome data (one bit per pixel) into a second color format which is n-bit per pixel during a moving operation.

The foreground color and background color is addressed respectively from I/O address 8290h to 8292h and from I/O address 8294h to 8296h. The font patterns are stored in the pattern registers (I/O address 82ACh to 82EBh) or in the off-screen memory which is called Enhanced Color/Font Expansion. These pattern registers store the monochrome bitmap. The BitBlt engine can expand 512 pixels at a time. Thus the font-drawing and monochrome bitmap expansion can be easily accomplished.

Enhanced Color Expansion

If the size of a monochrome bitmap is larger than 512 pixels, there is not enough space in pattern registers to store this bitmap. In this case, the bitmap should be stored in the off-screen display memory instead of the pattern registers. The operation is called Enhanced Color Expansion or Enhanced Font Expansion depended on the data format.

The format written into the off-screen memory of the Enhanced Color Expansion operation is $m \times n$.

When the Command 1 Register D[5] (Enhanced Color Expansion Enable Bit, I/O address 82ABh) is set to 1, the Enhanced Color Expansion mode is enable. The SRC Start Linear Address (I/O address 8280h to 8282h) is used to specify the starting address of the off-screen memory. Integrated Graphics Controller stores the monochrome bitmap into the assigned off-screen memory. Therefore the BitBlt engine could expand more pixels using the Enhanced Color Expansion.

Enhanced Font Expansion

The Enhanced Font Expansion is very similar to the Enhanced Color Expansion. The major difference is the format stored in the off-screen memory. The format written into the off-screen memory of the Enhanced Font Expansion operation is $8 \times n$.

When the Command 1 Register D[4] (Enhanced Font Expansion Enable Bit, I/O address 82ABh) is set to 1, the Enhanced Font Expansion mode is enable. The SRC Start Linear Address (I/O address 8280h to 8282h) is used to specify the start address of the off-screen memory. Integrated Graphics Controller stores the monochrome bitmap into off-screen memory byte by byte successively. Therefore the BitBlt engine would expand these pixels using the Enhanced Font Expansion.

Line Drawing

The Bresenham's Line Algorithm is a well popular algorithm in graphics, which is used to draw a line. The drawing line could be either a solid line or a dashed line. To draw a solid line, we must use one solid foreground color. To draw a dashed line, we'll use two colors specified by the foreground and background color registers. There are several registers involved to control the starting location, pixel count, error term, and line style, etc.



Rectangle Fill

A rectangle area fill is a function to fill a specified rectangle area by using either a solid color (rectangle fill) or a pattern (pattern fill).

Rectangle Fill is simply to fill the destination rectangle with a solid color. The solid color is specified into the foreground color register.

Pattern Fill repeats a source pattern into a destination rectangle. Therefore the pattern registers (I/O address 82ACh to 82EBh) must be specified. The pattern often consists of a background and foreground color because the color expansion would be used in conjunction with the pattern fill.

Raster Operations (Raster Ops or ROPs)

Raster Ops would perform some logical or arithmetic operations on the graphics data. There are 256 raster ops defined by Microsoft. Each raster op code is a Boolean operation with three operands: the source, the selected pattern, and the destination.

Direct Draw

The Windows 95 Game SDK enables the creation of world class computer games. Direct Draw is a component of that SDK that allows direct manipulation of video display memory. In order to enhance the performance of games, SiS 6205 provides some Direct Draw functions.

Since the former engine functions (from page 12 to page 14) can just support part of Direct Draw capabilities, three new functions are added into the graphics accelerator in order to meet the other Direct Draw functions. They are color key range comparison, alpha blending, and Direct Draw raster operation.

The register format for Direct Draw is different from those of the engine's functions listed above.

To enable Direct Draw, the Direct Draw enable bits (refer to "Command Register 1" on page 88) must be set to "11". Once Direct Draw is enabled, all of the engine operations are under the "Read-Modify-Write" mode. That is, the destination data have to be read from memory for processing before being written back.

After receiving the destination data, the source and destination data are sent to the color key range comparators to determine whether they are between the high and low color key values. If they are in the color key range, the Direct Draw raster operation (D_Rop) will determine whether the data after alpha blending or the original destination will be written back to memory.

There are two control bits for alpha blending. They are the S_Alpha bit (refer to "Alpha Blending Control Bit for Source Color" on page 95.) and D_alpha Bit (refer to "Alpha Blending Control Bit for Destination Color" on page 95.). The table below shows the relationship between these two control bits and the data after alpha blending.

| S_Alpha | D_Alpha | Data after Alpha Blending |
|---------|---------|--|
| 0 | 0 | Source |
| 0 | 1 | Destination |
| 1 | 0 | Source |
| 1 | 1 | $(\text{Source} + \text{Destination}) / 2$ |

3.1.10 PCI Bus Interface

SiS 6205 connects directly to the PCI bus with no glue logic, and it decodes the 32-bit address and responds to the applicable control lines. It could execute both I/O and memory access as an 8-, 16-, 32-bit device.

3.1.11 RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC.

The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital color value to three analog voltages for red, green, and blue.

3.1.12 Read-ahead Cache

It is a 128-bit cache. With this cache, the times of the operation of display memory read would be reduced, thus increase the performance.

3.1.13 Video Accelerator

SiS 6205 video accelerator could work in five different modes: standard FC (feature connector) mode, SiS FC (SiS Proprietary Defined Feature Connector) mode, direct video mode, VMI interface mode, and PCI multimedia mode.

In standard FC mode, SiS 6205 supports standard FC operation.

In SiS FC mode, SiS 6205 would co-operate with SiS 6204 MPEG and/or video adapter. After receiving the video data from SiS 6204, SiS 6205 would perform scaling and store these video data to display memory. Furthermore SiS 6205 would perform color-space conversion, interpolation, and scaling on the stored video data before overlaying with graphics data for final display. (For detailed video accelerator description, please refer to "3.10 Video Accelerator on page 21".)

The SiS proprietary defined feature connector are described in the next table:

| Symbol | FC Pin No. | Description |
|------------|------------|--|
| VIDEO[7:0] | 1-8 | <i>Video Data</i> The 8-bit video data format can be RGB 555, RGB 565, YUYV 422, YVYU 422, UYVY 422, VYUY 422 and Brooktree ByteStream™ format. |
| VDDE | 10 | <i>Video Data Valid</i> Active high signal When VDDE is high, the video data will be captured by SiS 6205. |
| PCLK | 9 | <i>Video pixel clock.</i> The video data output is based on PCLK. The frequency should be under 30MHz. |
| VDVSYNC | 18 | <i>Video Data Vertical Sync Signal</i> This signal is active when frame is change. The positive edge will be detected. |



| | | |
|---------|----|--|
| VDFIELD | 19 | <i>Video Data Field Signal</i> This signal indicates the current frame is odd or even frame. |
| EVIDEO | 17 | <i>Enable Video Data Input</i> Active low When this pin is low and the video controller is programmed to video capture mode, the video data can be transformed from Feature Connector or direct input by using the same signal definition. |

In direct video mode, SiS 6205 could work with the Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) to provide the PC-Video solution and provide the very flexible overlaying ability mentioned above.

In VMI interface mode, SiS 6205 could connect to some VMI devices.

In PCI multimedia mode, SiS 6205 supports PCI multimedia design specification to meet future potential trend.

3.1.14 Write FIFO

The Write FIFO contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. With this queue, the SiS 6205 will release CPU as soon as it records the address and data, and then write into display memory when the display memory is available. Thus CPU performance is increased.

3.2 BIOS ROM

SiS 6205 follows the One-Load-Per-Slot specification of PCI standard Revision 2.1. The address bus of BIOS ROM are multiplexed with MD[15:0] and the data bus are multiplexed with MD[23:16]. Note that this solution is without glue logic.

3.3 Bus Interface

The SiS 6205 dedicatedly supports 32-bit PCI Local Bus Standard Revision 2.1. Furthermore SiS 6205 supports PCI burst write to take advantage of PCI bus advanced feature to further improve performance. But PCI burst read is not supported since it has very little impact on performance in graphics application.

3.4 DRAM Support

SiS 6205 supports 1 MByte, 2 Mbyte, and 4 MByte FP DRAM and EDO DRAM configuration.

SiS 6205's signal interface can support IBM PS II 72-pin SIMM (single side & dual side). This will help vender to reduce the cost of the mass production for either all-in-one mainboard or graphics adapter card.

The FP DRAM and EDO DRAM types that SiS 6205 supports are: 256Kx4, 256Kx8, 1-CAS/2-WE 256Kx16, and 2-CAS/1-WE 256Kx16.

SiS 6205 also supports auto memory size detecting to provide more flexibility in mass production.



3.5 Video Memory Data Bus Architecture

The SiS 6205 uses the 64-bit DRAM data bus with peak video memory bandwidth of 220 MByte/sec for FP DRAM with 55Mhz MCLK and 320 MByte/sec for EDO DRAM with 80 Mhz MCLK.

In 2MByte DRAM configuration, SiS 6205 can support 1024x768x32K color, 1024x768x64K color, and 800x600x16M color resolutions with no degradation in the graphics performance.

In 4MByte DRAM configuration, SiS 6205 can support 1024x768x16M color, 1280x1024x32K color, and 1280x1024x64K color resolutions. These resolutions are not easily implemented by the regular Graphics Controller architecture.

3.5.1 Memory Configuration Pins

Under non-shared memory configuration (adapter mode),

In 1-bank configuration,

- RAS0* would be active.
- Only CASA[0:3]* (WEA[0:3]*¹) would be active.
- Only WEA* (CASA*¹) would be active.
- Only OE* would be active.
(OE* is designed for EDO DRAM. For normal DRAM, it is internal gated low.)
- Only MD[0:31] would be active.
- MAA0 and MAB0 are asserted and deasserted in the same time.
- MAA[1:7] would be connected to all bank.

In 2-bank configuration,

- RAS0* would be active.
- Only CASA[0:7]* (WEA[0:7]*¹) would be active.
- Only WEA* (CASA*¹) would be active.
- Only OE* would be active.
(OE* is designed for EDO DRAM. For normal DRAM, it is internal gated low.)
- MAA0 and MAB0 are asserted and deasserted in the same time.
- MAA[1:7] would be connected to all bank.

In 4-bank configuration,

- RAS0* would be active.
- CASA[0:7]* (WEA[0:7]*¹) and CASB[0:7]* (WEB[0:7]*¹) would be active.
- WEA* (CASA*¹) and WEB* (CASB*¹) would be active.
- Only OE* would be active.
(OE* is designed for EDO DRAM. For normal DRAM, it is internal gated low.)
- MAA0 and MAB0 would be active.
- MAA[1:7] would be connected to all bank.

Under shared memory configuration, refer to "3.11 Shared Memory on page 26".

OE* is used to support EDO (Extended Data Output) DRAM.

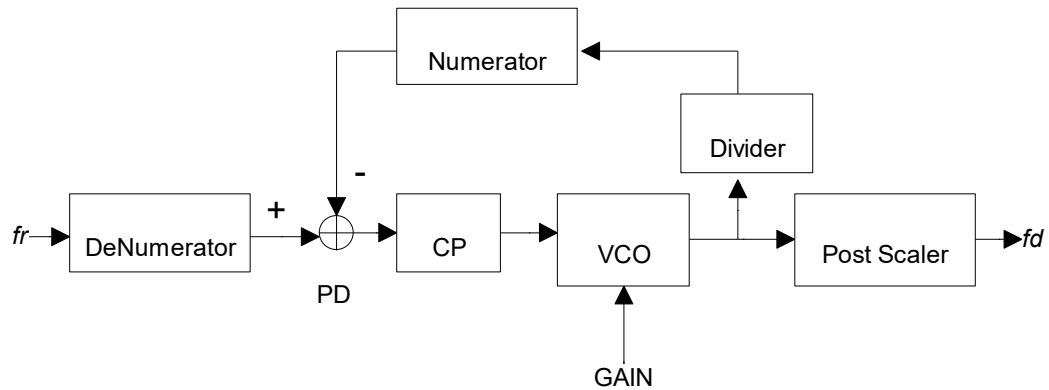
For recommended memory configuration layout (non-shared memory config.), please refer to Appendix A.

Note 1: For 2-WE/1-CAS 256Kx16 DRAM.

3.6 Internal Dual-Clock Synthesizer

SiS 6205 has built-in a dual-clock synthesizer to generate the MCLK and VCLK. This clock synthesizer could generate several variable frequencies, thus it could provide the flexibility for selecting the working frequency.

The following block diagram is for clock synthesizer.



where PD is **phase detection**,
 CP is **charge pump**,
 VCO is **voltage controlled oscillator**,
fr is **reference frequency**, and
fd is **desired frequency**.

The operation of clock synthesizer is described as follow:

When the synthesizer outputs the steady frequency, it means that

$$fr/DeNumerator = fd*Post\ Scalar / (Divider*Numerator).$$

i.e.

$$fd = fr * (Numerator/DeNumerator) * (Divider/Post\ Scalar).$$

With this formula, we could select adequate values for Numerator, DeNumerator, Divider, and Post Scalar to obtain the desired frequency.

The planned Video Clocks (VCLK) are as follow: (units: Mhz)

| | | | | |
|--------|---------|---------|---------|--------|
| 25.175 | 28.322 | 40.000 | 50.000 | 77.000 |
| 36.000 | 44.889 | 135.000 | 120.000 | 80.000 |
| 31.500 | 110.000 | 65.000 | 75.000 | 94.500 |

These frequencies are compatible with ICS2494-275 or -280.

Other video clocks would be added to the scheme after verified OK.

The planned Memory Clocks (MCLK) are from 50 MHz to 80 MHz with resolution 2 MHz. Higher memory clocks would be added after verified OK.



3.7 Power Management

To satisfy the power saving for Green PC, SiS 6205 supports the control protocol of DPMS (Display Power Management Signaling) proposed by VESA Monitor Committee. This protocol can reduce the VGA Monitors' power consumption.

SiS 6205 has built-in two timers for stand-by and suspend modes that can be programmed from 2 minutes to 30 minutes (2 min./increase) with the extended registers.

SiS 6205 also supports forcing the video subsystem into stand-by, suspend, or off modes with the extended registers.

Power saving is done by blocking HSYNC and/or VSYNC signals to the VGA monitor. The sources of activation are from the monitoring of keyboard, hardware cursor, and/or video memory read/write. The overview of the signal blocking requirements are as follows:

| POWER MANAGEMENT STATE | HORIZONTAL SYNC | VERTICAL SYNC | VIDEO DISPLAY |
|------------------------|-----------------|---------------|---------------|
| ON | Pulses | Pulses | Yes |
| Stand-By | No Pulses | Pulses | No |
| Suspend | Pulses | No Pulses | No |
| OFF | No Pulses | No Pulses | No |

3.8 Resolutions Supported

| Resolution | 1 MByte DRAM | 2 MByte DRAM | 4 MByte DRAM |
|--------------|--------------|--------------|--------------|
| 640x480x8 | √ | √ | √ |
| 640x480x16 | √ | √ | √ |
| 640x480x24 | √ | √ | √ |
| 800x600x4 | √ | √ | √ |
| 800x600x8 | √ | √ | √ |
| 800x600x16 | √ | √ | √ |
| 800x600x24 | X | √ | √ |
| 1024x768x4 | √ | √ | √ |
| 1024x768x8 | √ | √ | √ |
| 1024x768x16 | X | √ | √ |
| 1024x768x24 | X | X | √ |
| 1280x1024x4 | √ | √ | √ |
| 1280x1024x8 | X | √ | √ |
| 1280x1024x16 | X | X | √ |

Except these real resolution modes, SiS 6205 is also built-in virtual screen mode which could support up to 2048x2048 resolution.

3.9 Turbo Queue

In SiS 6205, the graphics engine performs the acceleration functions as stated in "Sec. 3.1.9 on page 12" via the acceleration commands stored in the command queue. The command queue is a FIFO (First In First Out) and ring structure. i.e. If an acceleration command is filled in the

last stage of the command queue, then the following acceleration command would be filled in the first stage of the command queue.

Once this command queue is congested, the CPU's request will be pending until the command queue has free space to accept more acceleration commands. This would downgrade the graphics system performance severely. Thus the length of command queue will dominate the performance of the graphics engine.

To lengthen the command queue as long as required, SiS 6205 provides two different kinds of command queue. The first one is built in SiS 6205, which is called *Hardware Command Queue*. The other one is built in the off-screen display memory, which is called *Turbo Queue*.

The Hardware Command Queue is a 32 doublewords queue built in front of the graphics engine. Since the average length of an engine command is 8 doublewords, it could be regarded as 5 stages command queue, the first one is in the active state and the last four are in the wait states.

The Turbo Queue is an extraordinary structure developed and **patent pending** by SiS Corp.

The system configuration of the two command queues and the graphics engine is shown in the following diagram.

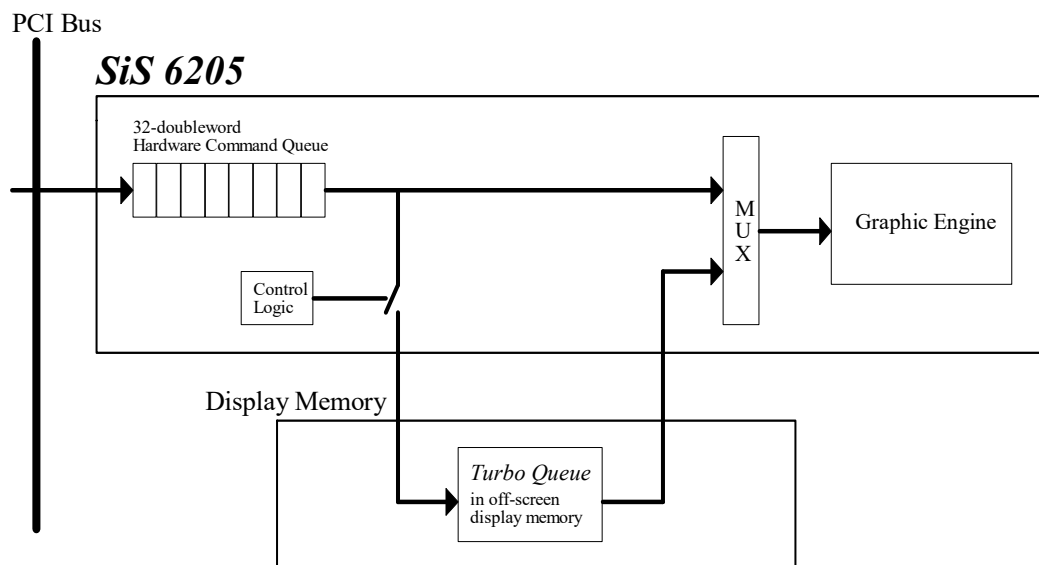


Figure 3.1 Turbo Queue Architecture

The Turbo Queue is also a FIFO and ring structure as stated before. The size of the Turbo Queue in SiS 6205 is 32K bytes. Thus the stages of graphics engine could be regarded as infinity. It could get rid of the disadvantages of the CPU waiting problems due to the limited length of command queue and It could get extra high graphics performance.

To program the extended register SR2C (Turbo Queue Base Address Register) could allocate the Turbo Queue into the off-screen region of the display memory automatically. Once the commands in the Hardware Command Queue were moved into the Turbo Queue, the free space in the Hardware Command Queue could be vacated to store the next acceleration



command and the condition of CPU waiting could be avoided. If both the command queues are not empty, the graphics engine would perform the commands in Turbo Queue first until Turbo Queue is empty.

3.10 Video Accelerator

3.10.1 Video Password/Identification Register

A video registers protection is implemented in the index 80h of CRT index register 3D4. To disable the protection, the software must first match the protection key value of 86h. If not match, read/write to any of the video associated registers are denied.

3.10.2 Video Play Back

SiS 6205 video accelerator could work in five different modes : standard FC (feature connector) mode, SiS proprietary defined FC (feature connector) mode, direct video mode, VMI interface mode, and PCI multimedia mode.

In SiS proprietary defined FC mode, SiS 6205 would receive RGB565 27MHz video data from SiS 6204, through feature connector, and allows on-screen video and graphics overlaying on a pixel-by-pixel basis.

SiS 6204 could work with the Philips SAA7110 and SGS-Thomson STi3400, STi3430 MPEG decoder to provide both PC-Video and MPEG solution.

SiS 6205 supports both interlaced or non-interlaced video format, so that SiS 6204 doesn't have to convert the interlaced video data into non-interlaced format. This can save the line buffer for translating video data from interlaced to non-interlaced format.

Overlaying occurs within programmable video extents based on a flexible color key and chroma key mechanism. By using the programmable filter, scalar, and DDA interpolation to the video data, SiS 6205 allows the video data to blend and overlay with the graphics data at the same rate.

In direct video mode, SiS 6205 could work with the Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2), to provide the PC-Video solution and provide the very flexible overlaying ability mentioned above.

In VMI interface mode, SiS 6205 could work with VMI device, such as SGS-Thomson STi3400, STi3430 MPEG decoder and sound card, etc.

In addition to the SiS proprietary video solution, SiS 6205 also supports the industry standard FC spec to provide a standard video link to the third-parties' video adapters.

Furthermore in PCI multimedia mode, SiS 6205 supports PCI multimedia design guide Rev. 1.0 spec to meet future potential trend.

3.10.3 Feature Connector Interface

As illustrated in "Sec. 2.3.4 SiS 6205 Video Accelerator Block Diagram" on page 9, an IBM standard feature connector interface is supported.

In standard feature connector mode, SiS 6205 would transfer the graphics data to the connected video adapter for overlay and can accept the video data from the connected video adapter.

However in SiS feature connector mode, SiS redefined the pin definition of the feature connector allowing SiS 6204 to pass the video data to SiS 6205. The passed video data format is RGB565 and the maximum data rate is 30 MByte/sec. The RGB565 data are 16-bit. SiS 6204 would transfer the 16-bit data by two successive bytes cycle. SiS 6205 would recover the data back to RGB565 format.

The data input/output direction of SiS 6205 is controlled by the ESYNC, EVDCLK, EVIDEO pins and is automatically controlled by BIOS.

3.10.4 Video Capture Window

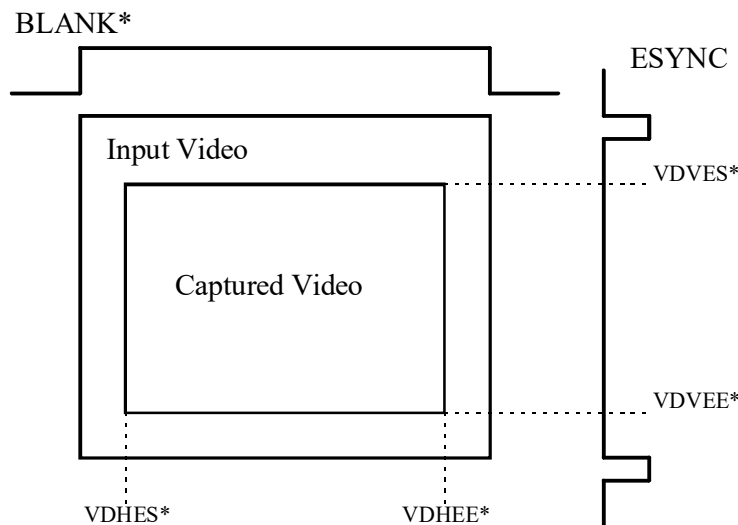


Figure 3.2

SiS 6205 provides video capture windowing to select a part of input video to be captured into video frame buffer. This capture window is defined by four parameter: video data horizontal start (VDHES), video data horizontal end (VDHEE), video data vertical start (VDVES), and video data vertical end (VDVEE).

There are the video data horizontal counter and the video data vertical counter inside SiS 6205. The video data horizontal counter is reset at the positive edge of signal BLANK* and counted up by PCLK or LLC1. The video data vertical counter is reset at the positive edge of ESYNC and counted up by positive of BLANK*. When the value of the video data horizontal counter is equal to or greater than VDHES and the video data vertical counter is equal to or greater than VDVES, the video data capture starts or continues. After the value of the video data horizontal counter is equal to or greater than VDHEE or the video data vertical counter is equal to or greater than VDVEE, the video capture ends.

3.10.5 Video Captured Down Scaling

SiS 6205 provides independent X-Y down scaling of the captured video image in integer increments of 1/64. Images may be scaled down to $n/64$ ($n = 1 \sim 64$) of the original image size to support video icons for graphics user interfaces, or to reduce the memory bandwidth. The scaling factor is controlled by HDSF and VDSF, which ranging from 0 to 63, and the scaling factors are $(64-HDSF)/64$ in horizontal and $(64-VHSF)/64$ in vertical.



3.10.6 Video Capture FIFO

The scaled-down video data would be fed into the video capture FIFO before being stored to display memory. The 64x16 video capture FIFOs serve as buffers between the video capture mechanisms and the display memory, are provided to fit the bandwidth limitation of the display memory during video image capture operation.

3.10.7 Multi-format Video Frame Buffer

The video frame buffer of SiS 6205 is shared with graphics frame buffer and is a multi-format frame buffer. It could accept 16-bpp YUV422, RGB555, and RGB565 color format.

The decompression CODEC, hardware or software, could fill the valid decompressed video frame data into the off-screen video frame buffer through the PCI local bus.

The other PCI motion video card or CPU can transfer the video data through PCI local bus directly into video frame buffer.

Then SiS 6205 would overlay the video on the screen.

3.10.8 Video Playback Line Buffers

When CRT refresh the screen, the video data must be overlaid with graphics data. Therefore the video data would first be read out from off-screen video frame buffer into the video playback line buffers for further handling.

The video playback line buffers serve as buffers between display memory and the playback mechanisms, are provided to fit the limitation of the display memory during video playback operation.

3.10.9 Color Space Conversion & Color Format Conversion

If the data read from the video frame buffer is in YUV422, the real time YUV-to-RGB converter will be turn on. The video data would be converted to RGB888 format for successive processing. The YUV422 are converted following the CCIR601-2 standard.

If the data read from the video frame buffer is in RGB format, the YUV-to-RGB converter would be bypassed. All the RGB565 and RGB555 format are supported and then would be converted to RGB888 format.

3.10.10 Horizontal Interpolation DDA

The DDA (Digital Differential Accumulator) using the following mathematical calculation with 2-tap, N-phase and scaling up factor UFACT (from J points scaling up to J * UFACT points):

$$\begin{aligned} \text{Destination}[i] &= (1 - \text{Weight}^n) * \text{Source}[j] + \text{Weight}^n * \text{Source}[j+1] \\ j &= \text{TRUNC}(i / \text{UFACT}) \\ \text{Weight}^n &= \text{TRUNC}(i / \text{UFACT}) - j \end{aligned}$$

However since the Weight^n is not an integer, the multiplication is hard to implement and therefore the following Weight is used for calculation.

$$\text{Weight} = \text{TRUNC}(\text{Weight}^n * 2^N) / 2^N$$

The SiS 6205 built-in an X-interpolation DDA mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

3.10.11 Vertical Interpolation DDA

The SiS 6205 built-in a Y-interpolation DDA mechanism and two line buffers mechanism to get better video stretching quality. The interpolation accuracy of DDA mechanism is 2-tap and 8-phase.

3.10.12 Video Playback Horizontal Zooming

The playback video data can be horizontal zoom-in in $64/n$ factor ($n = 1 \sim 64$) and zoom-out in about $m/16$ factor ($m = 1 \sim 16$). The zooming factor (HPFACT) is controlled by 4-bit integer part and 6-bit fraction part. The horizontal video size will be zoomed to $1/HPFACT$. If $HPFACT < 1$, it will performing horizontal up scaling. If $HPFACT > 1$, it will performing horizontal down scaling.

3.10.13 Video Playback Vertical Zooming

The playback video data can be vertical zoom-in in $64/n$ factor ($n = 1 \sim 64$) and zoom-out in arbitrary factor. The zooming factor (VPFACT) is controlled by 6-bit fraction part. The video size will be zoomed to $1/VPFACT$. Since the VPFACT is always less than 1, therefore you can only perform vertical up scaling by this factor. The vertical down scaling can be done by multiplying the Video Frame Buffer Offset with an integer I. Then the vertical video size will be zoomed to $1/(I*VPFACT)$.

3.10.14 Video Data Blending

The pixels of graphics data can be blended by graphics data alpha value, then add with the blended video data to generate blended data. The accuracy of the blending is 3 bits, the 3 MSBs of this register.

The pixels of video data can be blended by video data alpha value, then add with the blended graphics data to generate blended data. The accuracy of the blending is 3 bits, the 3 MSBs of this register.

3.10.15 Color Keying

A control signal is generated by comparing the 24 bits graphics data to the 24 bits color key low value and 24 bits color key high value. The bit number is dependent on color depth used. If the graphics data value is between the two color key values (all of three RGB parts), the color key is detected. This comparison mechanism can be disable by setting the video window size to zero, i.e. X-start=0, X-end=0, Y-start=0, and Y-end=0.

3.10.16 Chroma Keying

A control signal is generated by comparing the 24 bits video data to the 24 bits chroma key low value and 24-bit chroma key high value. The chroma key can be YUV or RGB format. If the video data value is between two chroma key values (all of three RGB or YUV parts), the chroma key is detected.

3.10.17 Graphics & Video Overlay

The overlay of the graphics data and the video data is performed by color keying and chroma keying method. The overlay operation is set by Key Overlay Operation Mode Register. The operation is defined below:



| Operation Mode | Operation |
|----------------|---|
| 0000 | always select graphics data |
| 0001 | select blended data when color key and chroma key, otherwise select graphics data |
| 0010 | select blended data when color key and not chroma key, otherwise select graphics data |
| 0011 | select blended data when color key, otherwise select graphics data |
| 0100 | select blended data when not color key and chroma key, otherwise select graphics data |
| 0101 | select blended data when chroma key, otherwise select graphics data |
| 0110 | select blended data when color key xor chroma key, otherwise select graphics data |
| 0111 | select blended data when color key or chroma key, otherwise select graphics data |
| 1000 | select blended data when not color key and not chroma key, otherwise select graphics data |
| 1001 | select blended data when color key xnor chroma key, otherwise select graphics data |
| 1010 | select blended data when not chroma key, otherwise select graphics data |
| 1011 | select blended data when color key or not chroma key, otherwise select graphics data |
| 1100 | select blended data when not chroma key, otherwise select graphics data |
| 1101 | select blended data when not color key or chroma key, otherwise select graphics data |
| 1110 | select blended data when not color key or not chroma key, otherwise select graphics data |
| 1111 | always select blended data |

3.10.18 Video Window Control Registers

The video window area is defined by six registers that specify a rectangular region by X-start, X-end, Y-start, and Y-end (X: Horizontal, Y: Vertical). Please refer to Sec 6.9.1~6.9.7 from page 100 to page 101.

The location of the video window is referenced to the VGA sync signals.

The size of the video window is defined in VGA pixels and lines.

3.10.19 Video Panning

The displayed video image could be panned around the captured video image by setting the video display starting address. i.e. You may selectively display any part of the captured video image. The video display starting address is equal to the video frame buffer starting address adds the panning offset. Please refer to Sec. 6.9.10~6.9.12.



3.10.20 Overlay Memory Data

The display memory is configured to two areas: one is the graphics area (which is the actual screen display area) storing graphics pixel data, and the other is the video area (which is also called off-screen area) storing the video pixel data.

In the graphics area, the corresponding video window area is reserved with the color key value. During the CRT scan period, a comparison of graphics data with color key data is performed. Once a match meet, the CRT output path would be switched from graphics path to video path to display the video data.

When the shared-memory architecture is used, the video frame buffer could be anywhere of the system memory, independent with the location of the graphics frame buffer. This provides more flexibility for video control application program. The video frame buffer should be set to non-cacheable and non-swappable.

3.11 Shared Memory

The SiS 6205 contains a scheme that allows DRAM memory access sharing among CPU and SiS 6205. This means the SiS 6205 can direct access the mother board DRAM which are allocated by BIOS. The SiS 6205 provides four interface signals: VGAREQ*, VGAREQH*, VGAGNT*, and HCLK to mother board chipset for hand shaking of DRAM access. There are three hand shaking modes provided: 2-wire 1-request, 2-wire 2-request, and 3-wire 2-request.

At reset cycle, the SiS 6205 will be set to shared memory mode if the VGAGNT* is deasserted. Otherwise the SiS 6205 will be set to non-shared memory mode.

In non-shared memory mode, the SiS 6205 will access the memory independent to VGAREQ* and VGAGNT*. In this case, the SiS 6205 must use its own display memory.

In shared memory mode, the system BIOS should setup the registers for shared memory, such as memory configuration, memory size, and memory bank, etc. So that the SiS 6205 can drive the correct RAS*, CASA*, CASB*, MA with selected **Scrambling Table**. The memory size can be 0.5MB, 1MB, 1.5MB, 2MB, 2.5MB, 3MB, 3.5MB, or 4MB with 32 bits or 64 bits DRAM. The DRAM refresh is completed by mother board chipset.

In shared-memory mode, the VGA BIOS could be combined with mother board BIOS. If using separate BIOS ROM, the VGA BIOS should be located in ISA bus. The SiS 6205 will generate VGAROMCS* and system will handle the BIOS read.

When SiS 6205 intend to access the DRAM, it asserts the VGAREQ*. The maximum latency time for mother board chipset to accept it and to assert VGAGNT* is about 600ns (at 1024 x 768 x 64k-color x 75Hz mode). The latency time is dependent on resolution, color depth, and frame rate.

The SiS 6205 provides three signals, VGAREQ* , VGAREQH*, and VGAGNT*, to chipset for hand shaking of DRAM access. Each signals are synchronized to HCLK. The handshaking protocol is as follows:

2-wire 1-request:

1. When SiS 6205 intend to access DRAM, it asserts VGAREQ*.
2. After VGAGNT* is asserted, the SiS 6205 starts to access DRAM.



3. The SiS 6205 completes the access and releases control to chipset. It first drives RAS*, CAS*, MA, and WE* for one clock and tri-state them. At the same time VGAREQ* is deasserted.
4. The VGAGNT* must be asserted at least two HCLK cycle.
5. The VGAREQ* will be deasserted at least two HCLK cycle.

2-wire 2-request:

1. When SiS 6205 intend to access DRAM, it asserts VGAREQ*.
If the DRAM cycle is CRT, video, or hardware cursor DRAM cycles, the SiS 6205 will deassert the VGAREQ* for one clock and then assert it again to acquire an higher priority request.
The chipset should assert the VGAGNT* as fast as possible when high priority request is asserted.
2. After VGAGNT* is asserted, the SiS 6205 starts to access DRAM.
3. The SiS 6205 completes the access and releases control to chipset. It first drives RAS*, CAS*, MA, and WE* for one clock and tri-state them. At the same time VGAREQ* is deasserted.
4. The VGAGNT* must be asserted at least two HCLK cycle.
5. The VGAREQ* will be deasserted at least two HCLK cycle.

3-wire 2-request:

1. When SiS 6205 intend to access DRAM for CRT, video, or hardware cursor DRAM cycles, it asserts VGAREQH.
When SiS 6205 intend to access DRAM for other cycles, it asserts VGAREQ*.
The chipset should assert the VGAGNT* as fast as possible when high priority request is asserted.
2. After VGAGNT* is asserted, the SiS 6205 starts to access DRAM.
3. The SiS 6205 completes the access and releases control to chipset. It first drives RAS*, CAS*, MA, and WE* for one clock and tri-state them. At the same time VGAREQ* is deasserted.
4. The VGAGNT* must be asserted at least two HCLK cycle.
5. The VGAREQ* will be deasserted at least two HCLK cycle.

Scrambling Table

| SCRAM Register Value | 0 | | 1 | | 2 | | 3 | |
|----------------------|-----------------|--------|---------------|--------|---------------|--------|----------------|--------|
| RAM type | 256K sym. 64bit | | 1M sym. 64bit | | 4M sym. 64bit | | 16M sym. 64bit | |
| MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA |
| 0 | 4 | 12 | 4 | 22 | 4 | 22 | 4 | 22 |
| 1 | 11 | 13 | 11 | 13 | 11 | 24 | 11 | 24 |
| 2 | 3 | 14 | 3 | 14 | 3 | 14 | 3 | 16 |
| 3 | 5 | 15 | 5 | 15 | 5 | 15 | 5 | 15 |
| 4 | 6 | 16 | 6 | 16 | 6 | 16 | 6 | 16 |
| 5 | 7 | 17 | 7 | 17 | 7 | 17 | 7 | 17 |
| 6 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 |
| 7 | 9 | 19 | 9 | 19 | 9 | 19 | 9 | 19 |



| | | | | | | | | |
|----|----|----|----|----|----|----|----|----|
| 8 | 10 | 20 | 10 | 20 | 10 | 20 | 10 | 20 |
| 9 | NA | NA | 12 | 21 | 12 | 21 | 12 | 21 |
| 10 | NA | NA | NA | NA | 13 | 23 | 13 | 23 |
| 11 | NA | NA | NA | NA | NA | NA | 14 | 25 |

| SCRAM Register Value | 4 | | 5 | | 6 | | 7 | |
|----------------------|------------------|--------|----------------|--------|----------------|--------|----------------|--------|
| RAM type | 512K asym. 64bit | | 1M asym. 64bit | | 2M asym. 64bit | | 4M asym. 64bit | |
| MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA |
| 0 | 4 | 12 | 4 | 12 | 4 | 22 | 4 | 22 |
| 1 | 11 | 13 | 11 | 13 | 11 | 13 | 11 | 13 |
| 2 | 3 | 14 | 3 | 14 | 3 | 14 | 3 | 14 |
| 3 | 5 | 15 | 5 | 15 | 5 | 15 | 5 | 15 |
| 4 | 6 | 16 | 6 | 16 | 6 | 16 | 6 | 16 |
| 5 | 7 | 17 | 7 | 17 | 7 | 17 | 7 | 17 |
| 6 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 |
| 7 | 9 | 19 | 9 | 19 | 9 | 19 | 9 | 19 |
| 8 | 10 | 20 | 10 | 20 | 10 | 20 | 10 | 20 |
| 9 | NA | 21 | NA | 21 | 12 | 21 | 12 | 21 |
| 10 | NA | NA | NA | 22 | NA | 23 | NA | 23 |
| 11 | NA | NA | NA | NA | NA | NA | NA | 24 |

| SCRAM Register Value | 8 | | 9 | | 10 | | 11 | |
|----------------------|-----------------|--------|---------------|--------|---------------|--------|----------------|--------|
| RAM type | 256k sym. 32bit | | 1M sym. 32bit | | 4M sym. 32bit | | 16M sym. 32bit | |
| MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA |
| 0 | 4 | 12 | 4 | 12 | 4 | 22 | 4 | 22 |
| 1 | 2 | 13 | 2 | 13 | 2 | 13 | 2 | 24 |
| 2 | 3 | 14 | 3 | 14 | 3 | 14 | 3 | 14 |
| 3 | 5 | 15 | 5 | 15 | 5 | 15 | 5 | 15 |
| 4 | 6 | 16 | 6 | 16 | 6 | 16 | 6 | 16 |
| 5 | 7 | 17 | 7 | 17 | 7 | 17 | 7 | 17 |
| 6 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 |
| 7 | 9 | 19 | 9 | 19 | 9 | 19 | 9 | 19 |
| 8 | 10 | 11 | 10 | 20 | 10 | 20 | 10 | 20 |
| 9 | NA | NA | 11 | 21 | 11 | 21 | 11 | 21 |
| 10 | NA | NA | NA | NA | 12 | 23 | 12 | 23 |
| 11 | NA | NA | NA | NA | NA | NA | 13 | 25 |

| SCRAM Register Value | 12 | | 13 | | 14 | | 15 | |
|----------------------|------------------|--------|---------------|--------|---------------|--------|----------------|--------|
| RAM type | 512K asym. 32bit | | 1M sym. 32bit | | 4M sym. 32bit | | 16M sym. 32bit | |
| MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA | Column MA | Row MA |
| 0 | 4 | 12 | 4 | 12 | 4 | 22 | 4 | 22 |
| 1 | 2 | 13 | 2 | 13 | 2 | 13 | 2 | 13 |
| 2 | 3 | 14 | 3 | 14 | 3 | 14 | 3 | 14 |
| 3 | 5 | 15 | 5 | 15 | 5 | 15 | 5 | 15 |
| 4 | 6 | 16 | 6 | 16 | 6 | 16 | 6 | 16 |
| 5 | 7 | 17 | 7 | 17 | 7 | 17 | 7 | 17 |
| 6 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 |
| 7 | 9 | 19 | 9 | 19 | 9 | 19 | 9 | 19 |
| 8 | 10 | 20 | 10 | 20 | 10 | 20 | 10 | 20 |
| 9 | NA | 11 | NA | 21 | 11 | 21 | 11 | 21 |
| 10 | NA | NA | NA | 11 | NA | 12 | NA | 23 |
| 11 | NA | NA | NA | NA | NA | NA | NA | 12 |

3.12 Signature Analysis

The signature analysis is provided to automatically test the graphics data which is the input of the DAC. This technique is based on the concept of cyclic redundancy checking (CRC) and is realized in hardware using linear feedback shift registers (LFSRs). It is composed of a 16-bit signature generator register which is called multiple-input signature register (*MISR*, shown in the following figure) and is used to ensure a unique signature of different patterns.

For a given test image, the signature analysis could get a right unique signature number. If an error occurs in the controller or the data manipulation, it would result in a different wrong signature number as compared to the pre-calculated signature value. Thus a test technician could sort the good or bad chips more quickly and accurately and requires no visual inspection of the screen for errors in the mass product environment. This could save significant testing time. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different when blink-off and blink-on for those frames. Assume all error patterns are equally likely, then the probability of failing to detect an error by the *MISR* is approximately 0.000015.

To match the inputs of *MISR*, the 24-bit graphics data (i.e. the input of the DAC of the RAMDAC) would be first converted into 16-bit data. The corresponding transfer function of the *MISR* of the following figure is

$$p(x) = 1 + c_1 \cdot x + c_2 \cdot x^2 + c_3 \cdot x^3 + \dots + c_{16} \cdot x^{16}$$

where $c_1, c_2, c_3, \dots, c_{16}$ can be either 0 or 1. SiS 6205 sets the parameters of the signature register as

$$p(x) = 1 + x + x^7 + x^{10} + x^{16}$$

Once the software enables the signature analysis function, SiS 6205 could test itself intelligently and automatically. This function could also be disabled by the extended control register for power saving purposes.

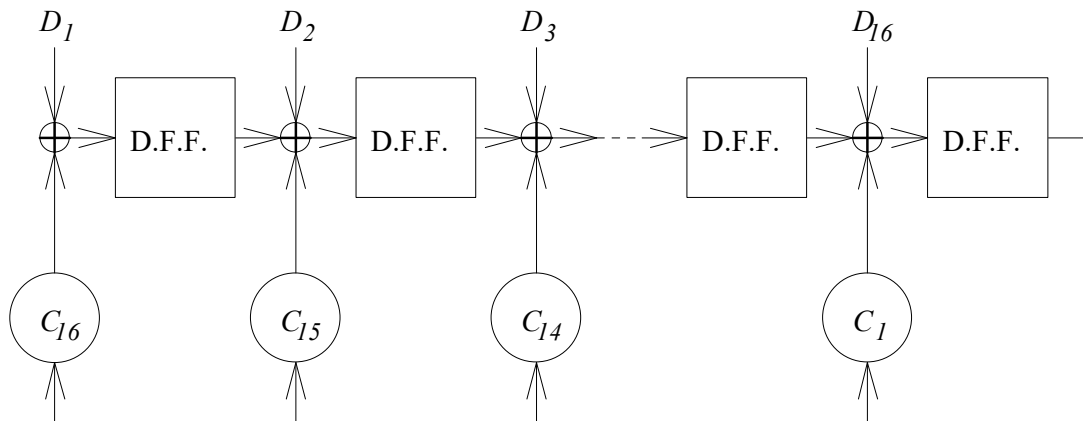


Figure 3.3 Multi-Input Signature Register (MISR)

3.13 Compatibility

The SiS 6205 is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes.

3.14 Software Support

To fully utilize and support the SiS 6205 hardware features, SiS has developed a high-performance VESA extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers developed by SiS. The following applications are currently supported:

- 3D Studio Ver. 3.0 & 4.0
- AutoCAD/386 Release 11, 12, 13
- Auto Shade/386 Ver. 2.0
- GEM 3.0/Ventura 2.0
- Lotus 1-2-3/Symphony Ver. 3.x
- MicroSoft Windows 3.1
- MicroSoft Windows 95
- MicroSoft Windows NT Ver. 3.1 & 3.5
- OrCad (SDT/VST/PCB) Rel 4
- OS/2 Presentation Manager 2.1 & 3.0
- P-CAD Ver. 6.06
- VersaCAD/386 Ver. 2.1
- Word Perfect 5.x & 6.0

Video operation are supported by software application drivers developed by SiS. The following applications are currently supported:

- Microsoft Video For Windows
- DCI driver
- Direct Draw driver



4. Pin Description

4.1 Pin Assignment

4.1.1 Pin Outline





4.1.2 Pin List

| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 1 | C/BE0 | I | |
| 2 | AD7 | I/O | 8R |
| 3 | AD6 | I/O | 8R |
| 4 | AD5 | I/O | 8R |
| 5 | AD4 | I/O | 8R |
| 6 | AD3 | I/O | 8R |
| 7 | AD2 | I/O | 8R |
| 8 | AD1 | I/O | 8R |
| 9 | AD0 | I/O | 8R |
| 10 | VSS | | |
| 11 | VGAREQ* | O | 4 |
| 12 | VGAGNT* | I | |
| 13 | HCLK | I | |
| 14 | RAS3* | O | 8 |
| 15 | RAS2* | O | 8 |
| 16 | RAS1* | O | 8 |
| 17 | MAA11 | O | 8R |
| 18 | MAA10 | O | 8R |
| 19 | VDD | | |
| 20 | CASB7* | I/O | 8 |
| 21 | CASB6* | I/O | 8 |
| 22 | CASB5* | I/O | 8 |
| 23 | CASB4* | I/O | 8 |
| 24 | MD63 | I/O | 4R, D |
| 25 | MD62 | I/O | 4R, D |
| 26 | MD61 | I/O | 4R, D |

| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 27 | MD60 | I/O | 4R, D |
| 28 | VSS | | |
| 29 | MD59 | I/O | 4R, D |
| 30 | MD58 | I/O | 4R, D |
| 31 | MD57 | I/O | 4R, D |
| 32 | MD56 | I/O | 4R, D |
| 33 | MD55 | I/O | 4R, D |
| 34 | MD54 | I/O | 4R, D |
| 35 | MD53 | I/O | 4R, D |
| 36 | MD52 | I/O | 4R, D |
| 37 | VDD | | |
| 38 | MD51 | I/O | 4R, D |
| 39 | MD50 | I/O | 4R, D |
| 40 | MD49 | I/O | 4R, D |
| 41 | MD48 | I/O | 4R, D |
| 42 | MAA9 | O | 8R |
| 43 | WEB* | O | 8 |
| 44 | MAB0 | O | 8R |
| 45 | MAA8 | O | 8R |
| 46 | MAA7 | O | 8R |
| 47 | MAA6 | O | 8R |
| 48 | VSS | | |
| 49 | MAA5 | O | 8R |
| 50 | MAA4 | O | 8R |
| 51 | MAA3 | O | 8R |
| 52 | MAA2 | O | 8R |

NOTE: Driving Type

8R: 8mA, 1 driven factor
8 : 8mA, 2 driven factor
4R: 4mA, 0.5 driven factor
4 : 4mA, 1 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down
U: Internal Pull-Up



| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 53 | AVSS2 | | |
| 54 | MFIL | A. I | |
| 55 | AVDD2 | | |
| 56 | VSS | | |
| 57 | MAA1 | O | 8R |
| 58 | MAA0 | O | 8R |
| 59 | CASB3* | I/O | 8 |
| 60 | CASB2* | I/O | 8 |
| 61 | CASB1* | I/O | 8 |
| 62 | CASB0* | I/O | 8 |
| 63 | PWDN* | I | |
| 64 | VDD | | |
| 65 | MD47 | I/O | 4R, D |
| 66 | MD46 | I/O | 4R, D |
| 67 | MD45 | I/O | 4R, D |
| 68 | MD44 | I/O | 4R, D |
| 69 | MD43 | I/O | 4R, D |
| 70 | MD42 | I/O | 4R, D |
| 71 | MD41 | I/O | 4R, D |
| 72 | MD40 | I/O | 4R, D |
| 73 | VSS | | |
| 74 | MD39 | I/O | 4R, D |
| 75 | MD38 | I/O | 4R, D |
| 76 | MD37 | I/O | 4R, D |
| 77 | MD36 | I/O | 4R, D |
| 78 | MD35 | I/O | 4R, D |

| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 79 | MD34 | I/O | 4R, D |
| 80 | MD33 | I/O | 4R, D |
| 81 | VDD | | |
| 82 | MD32 | I/O | 4R, D |
| 83 | WEA* | O | 8 |
| 84 | CASA7* | O | 8 |
| 85 | CASA6* | O | 8 |
| 86 | CASA5* | O | 8 |
| 87 | CASA4* | O | 8 |
| 88 | VSS | | |
| 89 | MD31 | I/O | 4R, D |
| 90 | MD30 | I/O | 4R, D |
| 91 | MD29 | I/O | 4R, D |
| 92 | MD28 | I/O | 4R, D |
| 93 | MD27 | I/O | 4R, D |
| 94 | MD26 | I/O | 4R, D |
| 95 | MD25 | I/O | 4R, D |
| 96 | MD24 | I/O | 4R, D |
| 97 | VDD | | |
| 98 | MD23 | I/O | 4R, D |
| 99 | MD22 | I/O | 4R, D |
| 100 | MD21 | I/O | 4R, D |
| 101 | MD20 | I/O | 4R, D |
| 102 | MD19 | I/O | 4R, D |
| 103 | MD18 | I/O | 4R, D |
| 104 | MD17 | I/O | 4R, D |

NOTE: Driving Type

8R: 8mA, 1 driven factor
8 : 8mA, 2 driven factor
4R: 4mA, 0.5 driven factor
4 : 4mA, 1 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down
U: Internal Pull-Up



| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 105 | MD16 | I/O | 4R, D |
| 106 | VSS | | |
| 107 | RAS0* | O | 8 |
| 108 | CASA3* | O | 8 |
| 109 | CASA2* | O | 8 |
| 110 | CASA1* | O | 8 |
| 111 | CASA0* | O | 8 |
| 112 | OEA* | O | 8 |
| 113 | VDD | | |
| 114 | MD15 | I/O | 4R, D |
| 115 | MD14 | I/O | 4R, D |
| 116 | MD13 | I/O | 4R, D |
| 117 | MD12 | I/O | 4R, D |
| 118 | MD11 | I/O | 4R, D |
| 119 | MD10 | I/O | 4R, D |
| 120 | MD9 | I/O | 4R, D |
| 121 | MD8 | I/O | 4R, D |
| 122 | VSS | | |
| 123 | MD7 | I/O | 4R, D |
| 124 | MD6 | I/O | 4R, D |
| 125 | MD5 | I/O | 4R, D |
| 126 | MD4 | I/O | 4R, D |
| 127 | MD3 | I/O | 4R, D |
| 128 | MD2 | I/O | 4R, D |
| 129 | MD1 | I/O | 4R, D |
| 130 | MD0 | I/O | 4R, D |

| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 131 | VDD | | |
| 132 | ROMCS* | O | 4R |
| 133 | VSYN | I/O | 8R |
| 134 | HSYN | I/O | 8R |
| 135 | BLANK* | I/O | 8 |
| 136 | PCLK | I/O | 8 |
| 137 | VIDEO7 | I/O | 8 |
| 138 | VIDEO6 | I/O | 8 |
| 139 | VIDEO5 | I/O | 8 |
| 140 | VIDEO4 | I/O | 8 |
| 141 | VIDEO3 | I/O | 8 |
| 142 | VIDEO2 | I/O | 8 |
| 143 | VIDEO1 | I/O | 8 |
| 144 | VIDEO0 | I/O | 8 |
| 145 | VSS | | |
| 146 | EVDCLK | I | U |
| 147 | ESYN | I | U |
| 148 | EVIDEO | I | U |
| 149 | AVSS | | |
| 150 | RSET | A. I | |
| 151 | COMP | A. I | |
| 152 | VREF | A. I | |
| 153 | ROUT | A. O | |
| 154 | GOUT | A. O | |
| 155 | BOUT | A. O | |
| 156 | AVDD | | |

NOTE: Driving Type
8R: 8mA, 1 driven factor
8 : 8mA, 2 driven factor
4R: 4mA, 0.5 driven factor
4 : 4mA, 1 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down
U: Internal Pull-Up



| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 157 | DDCDATA | I/O | 8R |
| 158 | DDCCLK | I/O | 8R |
| 159 | UVOE* | O | 4 |
| 160 | YOE* | O | 4 |
| 161 | GPIO | O | 4 |
| 162 | LLC1 | I | |
| 163 | VSS | | |
| 164 | INTA* | O | 8R |
| 165 | BARST* | I | |
| 166 | BCLK | I | |
| 167 | AD31 | I/O | 8R |
| 168 | AD30 | I/O | 8R |
| 169 | AD29 | I/O | 8R |
| 170 | AD28 | I/O | 8R |
| 171 | VDD | | |
| 172 | AD27 | I/O | 8R |
| 173 | AD26 | I/O | 8R |
| 174 | AD25 | I/O | 8R |
| 175 | AD24 | I/O | 8R |
| 176 | C/BE3 | I | |
| 177 | IDSEL | I | |
| 178 | AD23 | I/O | 8R |
| 179 | VSS | | |
| 180 | AD22 | I/O | 8R |
| 181 | AD21 | I/O | 8R |
| 182 | AD20 | I/O | 8R |

| Pin No. | Pin Name | Type | Driving Type |
|---------|----------|------|--------------|
| 183 | AD19 | I/O | 8R |
| 184 | AD18 | I/O | 8R |
| 185 | AD17 | I/O | 8R |
| 186 | AD16 | I/O | 8R |
| 187 | C/BE2 | I | |
| 188 | FRAME* | I | |
| 189 | IRDY* | I | |
| 190 | TRDY* | O | 8R |
| 191 | VDD | | |
| 192 | DEVSEL* | O | 8R |
| 193 | STOP* | O | 8R |
| 194 | C/BE1 | I | |
| 195 | PAR | I | |
| 196 | AD15 | I/O | 8R |
| 197 | AD14 | I/O | 8R |
| 198 | AD13 | I/O | 8R |
| 199 | AD12 | I/O | 8R |
| 200 | AD11 | I/O | 8R |
| 201 | AD10 | I/O | 8R |
| 202 | AD9 | I/O | 8R |
| 203 | AD8 | I/O | 8R |
| 204 | REFCLK | I | |
| 205 | VSS | | |
| 206 | AVDD1 | | |
| 207 | VFIL | A. I | |
| 208 | AVSS1 | | |

NOTE: Driving Type

8R: 8mA, 1 driven factor
8 : 8mA, 2 driven factor
4R: 4mA, 0.5 driven factor
4 : 4mA, 1 driven factor

A. I: Analog Input
A. O: Analog Output
D: Internal Pull-Down
U: Internal Pull-Up



4.2 Pin Definition

4.2.1 PCI Bus Interface

| Pin No. | Symbol | Type | Name and Function |
|---|---|------|---|
| 165 | BARST* | I | <i>PCI Reset</i> is used to bring PCI-specific registers, sequencer, and signals to a consistent state. |
| 166 | BCLK | I | <i>PCI Bus Clock</i> provides timing for all transactions on PCI bus. |
| 2~9, 196~203, 180~186, 178, 172~175, 167~170 | AD7~AD0, AD15~AD8, AD22~AD16, AD23, AD27~AD24, AD31~AD28 | I/O | <i>PCI Address/Data Bus</i> are multiplexed on the same pins. The Address phase is the clock cycle in which FRAME* is asserted and the data phase is immediately after the address phase. |
| 1, 194, 187, 176 | C/BE0, C/BE1, C/BE2, C/BE3 | I | <i>PCI Command/Byte Enable Bus</i> are multiplexed on the same pins. During the address phase of a transaction, C/BE define the bus command, and during the data phase C/BE are used as Byte Enables. |
| 195 | PAR | I | <i>PCI Parity Bit</i> is even parity across AD[31:0] and C/BE[3:0]. |
| 188 | FRAME* | I | <i>PCI Frame Cycle</i> is driven by the current master to indicate the beginning and duration of an access. |
| 190 | TRDY* | O | <i>PCI Target Ready</i> indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. |
| 189 | IRDY* | I | <i>PCI Initiator Ready</i> indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction |
| 193 | STOP* | O | <i>PCI Stop</i> indicates the current target is requesting the master to stop the current transaction. |
| 177 | IDSEL | I | <i>PCI Initialization Device Select</i> is used as a chip select during configuration read and write transactions. |
| 192 | DEVSEL* | O | <i>PCI Device Select</i> indicates whether any device on the bus has been selected. |
| 164 | INTA* | O | <i>PCI Interrupt</i> indicates the interrupt signal generated by SiS 6205. |

**4.2.2 Display Memory Interface**

| Pin No. | Symbol | Type | Name and Function |
|---|---|------|---|
| 14~16, 107 | RAS*[3:1], RAS0* | O | <i>Row Address Strobe</i> |
| 112 | OE* | O | <i>DRAM Output Enable</i> |
| 17,18, 42, 45~47, 49~52, 57 | MAA[11:10], MAA9, MAA[8:6], MAA[5:2], MAA1 | O | <i>Bank 0, 1, 2, 3 Memory Address bus</i> |
| 58 | MAA0 | O | <i>Bank 0, 1 Memory Address Bit[0]</i> |
| 44 | MAB0 | O | <i>Bank 2, 3 Memory Address Bit[0]</i> |
| 24~27, 29~52, 38~41, 65~72, 74~80, 82, 89~96, 98~105, 114~121, 123~130 | MD[63:60], MD[59:52], MD[51:48], MD[47:40], MD[39:33], MD32, MD[31:24], MD[23:16], MD[15:8], MD[7:0] | I/O | <i>Memory Data Bus</i> |

For all DRAM types except 1-CAS/2-WE DRAM,

| Pin No. | Symbol | Type | Name and Function |
|-------------------|--------------------------|------|---|
| 108~111, 84~87 | CASA[3:0]* CASA[7:4]* | O | <i>Bank 0, 1 Column Address Strobe bus</i> |
| 20~23, 59~62 | CASB[7:4]* CASB[3:0]* | O | <i>Bank 2, 3 Column Address Strobe bus, multiplexed with VIDEO[15:8]; It is used only for 64-bit interleave mode.</i> |
| 83 | WEA* | O | <i>Bank 0, 1 Write Enable</i> |
| 43 | WEB* | O | <i>Bank 2, 3 Write Enable</i> |

for 1-CAS/2-WE DRAM,

| Pin No. | Symbol | Type | Name and Function |
|-------------------|------------------------|------|--|
| 108~111, 84~87 | WEA[3:0]* WEA[7:4]* | O | <i>Bank 0, 1 Write Enable</i> |
| 20~23, 59~62 | WEB[7:4]* WEB[3:0]* | O | <i>Bank 2, 3 Write Enable</i> |
| 83 | CASA* | O | <i>Bank 0, 1 Column Address Strobe</i> |
| 43 | CASB* | O | <i>Bank 2, 3 Column Address Strobe</i> |

**4.2.3 Clock Control**

| Pin No. | Symbol | Type | Name and Function |
|---------|--------|------|--------------------------------|
| 204 | REFCLK | I | Reference Clock 14.318 MHz |
| 54 | MFIL | A. I | Memory Clock Filter |
| 208 | AVSS1 | | Analog Ground for Clock Gen. 1 |
| 206 | AVDD1 | | Analog Power for Clock Gen. 1 |
| 207 | VFIL | A. I | Video Clock Filter |
| 53 | AVSS2 | | Analog Ground for Clock Gen. 2 |
| 55 | AVDD2 | | Analog Power for Clock Gen. 2 |

NOTE: A. I: Analog Input; A. O: Analog Output

4.2.4 Video/Video DAC Interface (In Standard FC mode)

| Pin No. | Symbol | Type | Name and Function |
|---------|------------|------|---|
| 134 | HSYNC | I/O | Horizontal Sync |
| 133 | VSYNC | I/O | Vertical Sync |
| 136 | PCLK | I/O | Pixel Clock |
| 137~144 | VIDEO[7:0] | I/O | Video Data Bus |
| 135 | BLANK* | I/O | Blank Video signal |
| 153 | ROUT | A. O | Red Video Signal Output |
| 154 | GOUT | A. O | Green Video Signal Output |
| 155 | BOUT | A. O | Blue Video Signal Output |
| 151 | COMP | A. I | Compensation Pin Bypass this pin with an external 0.1 uF capacitor to AVDD. |
| 150 | RSET | A. I | Reference Resistor An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current. |
| 152 | VREF | A. I | Voltage Reference If an external voltage is used, it must supply this input with a 1.235V reference. |
| 147 | ESYNC | I | Enable Sync Input, active low |
| 146 | EVDCLK | I | Enable Video Clock Input, active low |
| 148 | EVIDEO | I | Enable Video Data Input, active low |

NOTE: A. I: Analog Input; A. O: Analog Output

4.2.5 Video Input Interface (In Direct Video Mode & SiS FC mode)

| Pin No. | Symbol | Type | Name and Function |
|---------|------------|------|---|
| 137~144 | VIDEO[7:0] | I/O | Video Data Bus |
| 160 | YOE* | O | Video Y signals output enable Mux with VMI VACTIVE, controlled by MD28 |
| 159 | UVOE* | O | Video UV signals output enable Mux with VMI VMICS*, controlled by MD28 |
| 162 | LLC1 | I | Video pixel clock Mux with VMI INTREQ, controlled by MD28 |



| | | | |
|-----|---------|-----|---|
| 147 | VDVSYNC | I | <i>Video Data Vertical Sync Signal, Mux with EVSYNC</i> |
| 146 | VDFIELD | I | <i>Video Data Field Signal, Mux with EVDCLK</i> |
| 148 | EVIDEO | I | <i>Enable Video Data Input, active low</i> |
| 135 | VDDE | I/O | <i>Video Data Valid</i> |
| 161 | GPIO | O | <i>General Purpose control pin</i> |

4.2.6 BIOS Interface

| Pin No. | Symbol | Type | Name and Function |
|----------------|---------------|-------------|--|
| 132 | ROMCS* | O | <i>ROM Chip Select</i> |
| | ROMADR[15:0] | I/O | <i>ROM Address Mux with MD[15:0]</i> |
| | ROMDAT[7:0] | I/O | <i>ROM Data Bus Mux with MD[23:16]</i> |

4.2.7 DDC Interface

| Pin No. | Symbol | Type | Name and Function |
|----------------|---------------|-------------|--|
| 157 | DDCDATA | I/O | <i>Display Data Channel Data Line</i> |
| 158 | DDCCLK | I/O | <i>Display Data Channel Clock Line</i> |

4.2.8 Shared Memory Interface

| Pin No. | Symbol | Type | Name and Function |
|----------------|---------------|-------------|---|
| 11 | VGAREQ* | O | <i>VGA shared memory request</i> |
| 132 | VGAREQH* | O | <i>VGA high priority shared memory request, Mux with ROMCS*</i> |
| 12 | VGAGNT* | I | <i>VGA shared memory grant</i> |
| 13 | HCLK | I | <i>CPU host clock</i> |

4.2.9 VMI Interface

| Pin No. | Symbol | Type | Name and Function |
|----------------|---------------|-------------|---|
| 162 | INTREQ | I | <i>VMI device interrupt request Mux with LLC1, controlled by MD28</i> |
| 159 | VMICS* | O | <i>VMI device csip select, active low Mux with YOE*, controlled by MD28</i> |
| 160 | VACTIVE | O | <i>VMI video active Mux with UVOE*, controlled by MD28</i> |

4.2.10 Misc.

| Pin No. | Symbol | Type | Name and Function |
|----------------|---------------|-------------|--------------------------------|
| 63 | PWDN* | I | <i>External Power Down Pin</i> |

4.2.11 Power and Ground

| Pin No. | Symbol | Type | Name and Function |
|----------------|---------------|-------------|--------------------------|
| 156 | AVDD | | <i>Analog Power</i> |
| 149 | AVSS | | <i>Analog Ground</i> |



| | | | |
|--|-----|--|-----------------------|
| 19, 37, 64, 81, 97,113, 131, 171, 191 | VDD | | <i>Digital Power</i> |
| 10, 28, 48, 56, 73, 88, 106, 122, 145, 163, 179, 205 | VSS | | <i>Digital Ground</i> |



5. Mode Tables

5.1 Standard VGA Modes

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|------|------|--------------|---------------|--------------|--------------|----------|------------|
| 0 | A/N | 320x200 | 16 | 40x25 | B800 | 8x8 | 8 |
| 0* | A/N | 320x350 | 16 | 40x25 | B800 | 8x14 | 8 |
| 0+ | A/N | 360x400 | 16 | 40x25 | B800 | 9x16 | 8 |
| 1 | A/N | 320x200 | 16 | 40x25 | B800 | 8x8 | 8 |
| 1* | A/N | 320x350 | 16 | 40x25 | B800 | 8x14 | 8 |
| 1+ | A/N | 360x400 | 16 | 40x25 | B800 | 9x16 | 8 |
| 2 | A/N | 640x200 | 16 | 80x25 | B800 | 8x8 | 8 |
| 2* | A/N | 640x350 | 16 | 80x25 | B800 | 8x14 | 8 |
| 2+ | A/N | 720x400 | 16 | 80x25 | B800 | 9x16 | 8 |
| 3 | A/N | 640x200 | 16 | 80x25 | B800 | 8x8 | 8 |
| 3* | A/N | 640x350 | 16 | 80x25 | B800 | 8x14 | 8 |
| 3+ | A/N | 720x400 | 16 | 80x25 | B800 | 9x16 | 8 |
| 4 | APA | 320x200 | 4 | 40x25 | B800 | 8x8 | 1 |
| 5 | APA | 320x200 | 4 | 40x25 | B800 | 8x8 | 1 |
| 6 | APA | 640x200 | 2 | 80x25 | B800 | 8x8 | 1 |
| 7 | A/N | 720x350 | 4 | 80x25 | B000 | 9x14 | 8 |
| 7+ | A/N | 720x400 | 4 | 80x25 | B000 | 9x16 | 8 |
| 0D | APA | 320x200 | 16 | 40x25 | A000 | 8x8 | 8 |
| 0E | APA | 640x200 | 16 | 80x25 | A000 | 8x8 | 4 |
| 0F | APA | 640x350 | 2 | 80x25 | B000 | 8x14 | 2 |
| 10 | APA | 640x350 | 16 | 80x25 | A000 | 8x14 | 2 |
| 11 | APA | 640x480 | 2 | 80x30 | A000 | 8x16 | 1 |
| 12 | APA | 640x480 | 16 | 80x30 | A000 | 8x16 | 1 |
| 13 | APA | 320x200 | 256 | 40x25 | A000 | 8x8 | 1 |

NOTE: 1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)



| MODE | DISPLAY SIZE | COLORS SHADES | FRAME RATE. | H-SYNC. | VIDEO FREQ. |
|------|--------------|---------------|-------------|---------|-------------|
| 0 | 320x200 | 16 | 70 | 31.5 K | 25.1 M |
| 0* | 320x350 | 16 | 70 | 31.5 K | 25.1 M |
| 0+ | 360x400 | 16 | 70 | 31.5 K | 28.3 M |
| 1 | 320x200 | 16 | 70 | 31.5 K | 25.1 M |
| 1* | 320x350 | 16 | 70 | 31.5 K | 25.1 M |
| 1+ | 360x400 | 16 | 70 | 31.5 K | 28.3 M |
| 2 | 640x200 | 16 | 70 | 31.5 K | 25.1 M |
| 2* | 640x350 | 16 | 70 | 31.5 K | 25.1 M |
| 2+ | 720x400 | 16 | 70 | 31.5 K | 28.3 M |
| 3 | 640x200 | 16 | 70 | 31.5 K | 25.1 M |
| 3* | 640x350 | 16 | 70 | 31.5 K | 25.1 M |
| 3+ | 720x400 | 16 | 70 | 31.5 K | 28.3 M |
| 4 | 320x200 | 4 | 70 | 31.5 K | 25.1 M |
| 5 | 320x200 | 4 | 70 | 31.5 K | 25.1 M |
| 6 | 640x200 | 2 | 70 | 31.5 K | 25.1 M |
| 7* | 720x350 | 4 | 70 | 31.5 K | 28.3 M |
| 7+ | 720x400 | 4 | 70 | 31.5 K | 28.3 M |
| 0D | 320x200 | 16 | 70 | 31.5 K | 25.1 M |
| 0E | 640x200 | 16 | 70 | 31.5 K | 25.1 M |
| 0F | 640x350 | 2 | 70 | 31.5 K | 25.1 M |
| 10 | 640x350 | 16 | 70 | 31.5 K | 25.1 M |
| 11 | 640x480 | 2 | 60 | 31.5 K | 25.1 M |
| 12 | 640x480 | 16 | 60 | 31.5 K | 25.1 M |
| 13 | 320x200 | 256 | 70 | 31.5 K | 25.1 M |

NOTE: i - interlaced mode
n - noninterlaced mode



5.2 Enhanced Video Modes

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|------|------|--------------|---------------|--------------|--------------|----------|------------|
| 22 | A/N | 1056x352 | 16 | 132x44 | B800 | 8x8 | 2 |
| 23 | A/N | 1056x350 | 16 | 132x25 | B800 | 8x14 | 4 |
| 24 | A/N | 1056x364 | 16 | 132x28 | B800 | 8x13 | 4 |
| 25 | APA | 640x480 | 16 | 80x60 | A000 | 8x8 | 1 |
| 26 | A/N | 720x480 | 16 | 80x60 | B800 | 9x8 | 3 |
| 29 | APA | 800x600 | 16 | 100x37 | A000 | 8x16 | 1 |
| 2A | A/N | 800x600 | 16 | 100x40 | B800 | 8x15 | 4 |
| 2D | APA | 640x350 | 256 | 80x25 | A000 | 8x14 | 1 |
| 2E | APA | 640x480 | 256 | 80x30 | A000 | 8x16 | 1 |
| 2F | APA | 640x400 | 256 | 80x25 | A000 | 8x16 | 1 |
| 30 | APA | 800x600 | 256 | 100x37 | A000 | 8x16 | 1 |
| 37 | APA | 1024x768 | 16 | 128x48 | A000 | 8x16 | 1 |
| 38 | APA | 1024x768 | 256 | 128x48 | A000 | 8x16 | 1 |
| 39 | APA | 1280x1024 | 16 | 160x64 | A000 | 8x16 | 1 |
| 3A | APA | 1280x1024 | 256 | 160x64 | A000 | 8x16 | 1 |
| 40 | APA | 320x200 | 32K | 40x25 | A000 | 8x8 | 1 |
| 41 | APA | 320x200 | 64K | 40x25 | A000 | 8x8 | 1 |
| 42 | APA | 320x200 | 16.8M | 40x25 | A000 | 8x8 | 1 |
| 43 | APA | 640x480 | 32K | 80x30 | A000 | 8x16 | 1 |
| 44 | APA | 640x480 | 64K | 80x30 | A000 | 8x16 | 1 |
| 45 | APA | 640x480 | 16.8M | 80x30 | A000 | 8x16 | 1 |
| 46 | APA | 800x600 | 32K | 100x37 | A000 | 8x16 | 1 |
| 47 | APA | 800x600 | 64K | 100x37 | A000 | 8x16 | 1 |
| 48 | APA | 800x600 | 16.8M | 100x37 | A000 | 8x16 | 1 |
| 49 | APA | 1024x768 | 32K | 128x48 | A000 | 8x16 | 1 |
| 4A | APA | 1024x768 | 64K | 128x48 | A000 | 8x16 | 1 |
| 4B | APA | 1024x768 | 16.8M | 128x48 | A000 | 8x16 | 1 |
| 4C | APA | 1280x1024 | 32K | 160x64 | A000 | 8x16 | 1 |
| 4D | APA | 1280x1024 | 64K | 160x64 | A000 | 8x16 | 1 |

- NOTE:** 1. A/N: Alpha/Numeric
2. APA: All Point Addressable (Graphics)



| MODE | DISPLAY SIZE | COLORS SHADES | FRAME RATE. | H-SYNC. | VIDEO FREQ. |
|-------------|---------------------|----------------------|--------------------|----------------|--------------------|
| 22 | 1056x352 | 16 | 70 | 30.5 K | 40.0 M |
| 23 | 1056x350 | 16 | 70 | 30.5 K | 40.0 M |
| 24 | 1056x364 | 16 | 70 | 30.5 K | 40.0 M |
| 25 | 640x480 | 16 | 60 | 31.5 K | 25.1 M |
| 26 | 720x480 | 16 | 60 | 31.5 K | 25.1 M |
| 29 | 800x600 | 16 | 56 | 35.1 K | 30.0 M |
| 29* | 800x600 | 16 | 60 | 37.9 K | 40.0 M |
| 29+ | 800x600 | 16 | 72 | 48.0 K | 50.0 M |
| 29# | 800x600 | 16 | 75 | 46.8 K | 50.0 M |
| 29### | 800x600 | 16 | 85 | 53.7 K | 56.3 M |
| 2A | 800x600 | 16 | 56 | 35.1 K | 36.0 M |
| 2D | 640x350 | 256 | 70 | 31.5 K | 25.1 M |
| 2E | 640x480 | 256 | 60 | 31.5 K | 25.1 M |
| 2E* | 640x480 | 256 | 72 | 37.9 K | 31.5 M |
| 2E+ | 640x480 | 256 | 75 | 37.5 K | 31.5 M |
| 2E++ | 640x480 | 256 | 85 | 43.4 K | 36.0 M |
| 2F | 640x400 | 256 | 70 | 31.5 K | 25.1 M |
| 30 | 800x600 | 256 | 56 | 35.1 K | 36.0 M |
| 30* | 800x600 | 256 | 60 | 37.9 K | 40.0 M |
| 30+ | 800x600 | 256 | 72 | 48.0 K | 50.0 M |
| 30# | 800x600 | 256 | 75 | 46.8 K | 50.0 M |
| 30### | 800x600 | 256 | 85 | 53.7 K | 56.3 M |
| 37i | 1024x768 | 16 | 87 | 35.5 K | 44.9 M |
| 37n | 1024x768 | 16 | 60 | 48.4 K | 65.0 M |
| 37n+ | 1024x768 | 16 | 70 | 56.5 K | 75.0 M |
| 37n# | 1024x768 | 16 | 75 | 60.2 K | 80.0 M |
| 37n### | 1024x768 | 16 | 85 | 68.7 K | 94.5 M |
| 38i | 1024x768 | 256 | 87 | 35.5 K | 44.9 M |
| 38n | 1024x768 | 256 | 60 | 48.4 K | 65.0 M |
| 38n+ | 1024x768 | 256 | 70 | 56.5 K | 75.0 M |
| 38n# | 1024x768 | 256 | 75 | 60.2 K | 80.0 M |
| 38n### | 1024x768 | 256 | 85 | 68.7 K | 94.5 M |
| 39i | 1280x1024 | 16 | 87 | 48.8 K | 80.0 M |
| 39n | 1280x1024 | 16 | 60 | 65.0 K | 110.0 M |
| 39n+ | 1280x1024 | 16 | 75 | 80.0 K | 135.0 M |
| 3Ai | 1280x1024 | 256 | 87 | 48.8 K | 80.0 M |
| 3An | 1280x1024 | 256 | 60 | 65.0 K | 110.0 M |
| 3An+ | 1280x1024 | 256 | 75 | 80.0 K | 135.0 M |



| | | | | | |
|-------|----------|-------|----|--------|--------|
| 40 | 320x200 | 32K | 70 | 31.5 K | 25.1 M |
| 41 | 320x200 | 64K | 70 | 31.5 K | 25.1 M |
| 42 | 320x200 | 16.8M | 70 | 31.5 K | 25.1 M |
| 43 | 640x480 | 32K | 60 | 31.5 K | 25.1 M |
| 43* | 640x480 | 32K | 72 | 37.9 K | 31.5 M |
| 43+ | 640x480 | 32K | 75 | 37.5 K | 31.5 M |
| 43++ | 640x480 | 32K | 85 | 43.4 K | 36.0 M |
| 44 | 640x480 | 64K | 60 | 31.5 K | 25.1 M |
| 44* | 640x480 | 64K | 72 | 37.9 K | 31.5 M |
| 44+ | 640x480 | 64K | 75 | 37.5 K | 31.5 M |
| 44++ | 640x480 | 64K | 85 | 43.4 K | 36.0 M |
| 45 | 640x480 | 16.8M | 60 | 31.5 K | 25.1 M |
| 45* | 640x480 | 16.8M | 72 | 37.9 K | 31.5 M |
| 45+ | 640x480 | 16.8M | 75 | 37.5 K | 31.5 M |
| 45++ | 640x480 | 16.8M | 85 | 43.4 K | 36.0 M |
| 46 | 800x600 | 32K | 56 | 35.1 K | 36.0 M |
| 46* | 800x600 | 32K | 60 | 37.9 K | 40.0 M |
| 46+ | 800x600 | 32K | 72 | 48.0 K | 50.0 M |
| 46# | 800x600 | 32K | 75 | 46.8 K | 50.0 M |
| 46## | 800x600 | 32K | 85 | 53.7 K | 56.3 M |
| 47 | 800x600 | 64K | 56 | 35.1 K | 36.0 M |
| 47* | 800x600 | 64K | 60 | 37.9 K | 40.0 M |
| 47+ | 800x600 | 64K | 72 | 48.0 K | 50.0 M |
| 47# | 800x600 | 64K | 75 | 46.8 K | 50.0 M |
| 47## | 800x600 | 64K | 85 | 53.7 K | 56.3 M |
| 48 | 800x600 | 16.8M | 56 | 35.1 K | 36.0 M |
| 48* | 800x600 | 16.8M | 60 | 37.9 K | 40.0 M |
| 48+ | 800x600 | 16.8M | 72 | 48.0 K | 50.0 M |
| 48# | 800x600 | 16.8M | 75 | 46.8 K | 50.0 M |
| 48## | 800x600 | 16.8M | 85 | 53.7 K | 56.3 M |
| 49i | 1024x768 | 32K | 87 | 35.5 K | 44.9 M |
| 49n | 1024x768 | 32K | 60 | 48.4 K | 65.0 M |
| 49n+ | 1024x768 | 32K | 70 | 56.5 K | 75.0 M |
| 49n# | 1024x768 | 32K | 75 | 60.2 K | 80.0 M |
| 49n## | 1024x768 | 32K | 85 | 68.7 K | 94.5 M |
| 4Ai | 1024x768 | 64K | 87 | 35.5 K | 44.9 M |
| 4An | 1024x768 | 64K | 60 | 48.4 K | 65.0 M |
| 4An+ | 1024x768 | 64K | 70 | 56.5 K | 75.0 M |
| 4An# | 1024x768 | 64K | 75 | 60.2 K | 80.0 M |
| 4An## | 1024x768 | 64K | 85 | 68.7 K | 94.5 M |



| | | | | | |
|-------|-----------|-------|----|--------|--------|
| 4Bi | 1024x768 | 16.8M | 87 | 35.5 K | 44.9 M |
| 4Bn | 1024x768 | 16.8M | 60 | 48.4 K | 65.0 M |
| 4Bn+ | 1024x768 | 16.8M | 70 | 56.5 K | 75.0 M |
| 4Bn# | 1024x768 | 16.8M | 75 | 60.2 K | 80.0 M |
| 4Bn## | 1024x768 | 16.8M | 85 | 68.7 K | 94.5 M |
| 4Ci | 1280x1024 | 32K | 89 | 48.8 K | 80.0 M |
| 4Di | 1280x1024 | 64K | 89 | 48.8 K | 80.0 M |

NOTE: i - interlaced mode
n - noninterlaced mode

- For the limitation of memory bandwidth in 1MB DRAM configuration, the following video modes is not supported in 1MB configuration: modes 45*, 45+, 46+, 46#, 47+, and 47#.



6. Registers Description

- 6.1 to 6.6 are IBM VGA standard registers.
- 6.7 to 6.9 are SiS 6205 Extended Registers.
- 6.10 is PCI configuration registers.

6.1 General Registers

6.1.1 Miscellaneous Output Register

Register Type: Read/Write
 Read Port: 3CC
 Write Port: 3C2
 Default: 00h

D7 Vertical Sync Polarity
 0: Select 'positive vertical sync'
 1: Select 'negative vertical sync'

D6 Horizontal Sync Polarity
 0: Select 'positive horizontal sync'
 1: Select 'negative horizontal sync'

Sync Polarity vs. Vertical Screen Resolution

| D7 | D6 | EGA | VGA |
|----|----|-----------|-----------|
| 0 | 0 | 200 Lines | Invalid |
| 0 | 1 | 350 Lines | 400 Lines |
| 1 | 0 | Invalid | 350 Lines |
| 1 | 1 | Invalid | 480 Lines |

D5 Odd/Even Page
 0: Select low page of memory
 1: Select high page of memory

D4 Reserved

D[3:2] Clock Select

Table for Video Clock Selection

| D3 | D2 | FS[3:0] |
|----|----|--|
| 0 | 0 | 0000 (25.175 MHz) |
| 0 | 1 | 0001 (28.322 MHz) |
| 1 | 0 | Don't Care |
| 1 | 1 | For external clock, refer to 6.7.4 Extended Registers, Index_07h D[3:0] on page 72. For internal clock generator, it's don't care. |

D1 Display RAM Enable
 0: Disable processor access to video RAM
 1: Enable processor access to video RAM

D0 I/O Address Select
 0: Sets addresses for monochrome emulation
 1: Sets addresses for color graphics emulation

**6.1.2 Feature Control Register**

Register Type: Read/Write

Read Port: 3CA

Write Port: 3BA/3DA

Default: 00h

D[7:4] Reserved (0)

D3 Vertical Sync Select

0: Normal Vertical Sync output to monitor

1: [Vertical Sync OR Vertical Display Enable] output to monitor

D[2:0] Reserved (0)

6.1.3 Input Status Register 0

Register Type: Read only

Read Port: 3C2

Default: 00h

D7 Vertical Retrace Interrupt Pending

0: Cleared

1: Pending

D[6:5] Reserved

D4 Switch Sense

D[3:0] Reserved

6.1.4 Input Status Register 1

Register Type: Read only

Read Port: 3BA/3DA

Default: 00h

D[7:6] Reserved

D[5:4] Diagnostic

Table for Video Read-back Through Diagnostic Bit (I)

| Color Plane Enable Register | | Input Status Register 1 | |
|-----------------------------|----|-------------------------|-----------------|
| D5 | D4 | D5 | D4 |
| 0 | 0 | Red | Blue |
| 0 | 1 | Secondary Red | Secondary Green |
| 1 | 0 | Secondary Blue | Green |
| 1 | 1 | Unused | Unused |

**Table for Video Read-back Through Diagnostic Bit (II)**

| Color Plane Enable Register | | Input Status Register 1 | |
|-----------------------------|----|-------------------------|----|
| D5 | D4 | D5 | D4 |
| 0 | 0 | P2 | P0 |
| 0 | 1 | P5 | P4 |
| 1 | 0 | P3 | P1 |
| 1 | 1 | P7 | P6 |

D3 Vertical Retrace
 0: Inactive
 1: Active
 D[2:1] Reserved
 D0 Display Enable Not
 0: Display period
 1: Retrace period

6.1.5 VGA Enable Register

Register Type: Read/Write
 Read/Write Port: 3C3 or 46E8
 Default: 00h
 D0 VGA Enable (for 3C3 only)
 0: Disable
 1: Enable
 D3 VGA Enable (for 46E8 only)
 0: Disable
 1: Enable

6.1.6 Segment Selection Register 0

Register Type: Read/Write
 Read/Write Port: 3CD
 Default: 00h

 If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then
 D[7:6] Reserved
 D[5:0] Segment Selection Write Bit[5:0]

 If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then
 D[7:6] Reserved
 D[5:3] Segment Selection Write Bit[2:0]
 D[2:0] Segment Selection Read Bit[2:0]



6.1.7 Segment Selection Register 1

Register Type: Read/Write
Read/Write Port: 3CB
Default: 00h

If D3 of SRB (Dual Segment Mode Enable bit) sets to 1, then

D[7:6] Reserved

D[5:0] Segment Selection Read Bit[5:0]

If D3 of SRB (Dual Segment Mode Enable bit) sets to 0, then

D[7:0] Reserved



6.2 CRT Controller Registers

6.2.1 CRT Controller Index Register

Register Type: Read/Write

Read/Write Port: 3B4/3D4

Default: 00h

D[7:5] Reserved

D[4:0] CRT Controller Index

- 00h ~ 18h for standard VGA

- 19h ~ 26h for SiS extended registers

| Index (3B4/3D4) | CRT Controller Registers (3B5/3D5) |
|-----------------|---|
| 0h | Horizontal Total |
| 1h | Horizontal Display Enable End |
| 2h | Horizontal Blank Start |
| 3h | Horizontal Blank End |
| 4h | Horizontal Retrace Start |
| 5h | Horizontal Retrace End |
| 6h | Vertical Total |
| 7h | Overflow Register |
| 8h | Preset Row Scan |
| 9h | Max Scan Line/Text Character Height |
| Ah | Text Cursor Start |
| Bh | Text Cursor End |
| Ch | Screen Start Address High |
| Dh | Screen Start Address Low |
| Eh | Text Cursor Location High |
| Fh | Text Cursor Location Low |
| 10h | Vertical Retrace Start |
| 11h | Vertical Retrace End |
| 12h | Vertical Display Enable End |
| 13h | Screen Offset |
| 14h | Underline Location |
| 15h | Vertical Blank Start |
| 16h | Vertical Blank End |
| 17h | Mode Control |
| 18h | Line Compare |
| 19h | Extended Signature Read-Back Register 0 |
| 1Ah | Extended Signature Read-Back Register 1 |
| 22h | Graphics Data Latch Readback Register |
| 24h | Attribute Controller Toggle Readback Register |
| 26h | Attribute Controller Index Readback Register |

**6.2.2 CR0: Horizontal Total**

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 00h
Default: 00h

D[7:0] Horizontal Total Bit[7:0]

6.2.3 CR1: Horizontal Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 01h
Default: 00h

D[7:0] Horizontal Display Enable End Bit[7:0]

6.2.4 CR2: Horizontal Blank Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 02h
Default: 00h

D[7:0] Horizontal Blank Start Bit[7:0]

6.2.5 CR3: Horizontal Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 03h
Default: 00h

D7 Reserved
D[6:5] Display Skew Control Bit[1:0]
00: No skew
01: Skew 1 character
10: Skew 2 characters
11: Skew 3 characters

D[4:0] Horizontal Blank End Bit[4:0]

6.2.6 CR4: Horizontal Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 04h
Default: 00h

D[7:0] Horizontal Retrace Start Bit[7:0]

6.2.7 CR5: Horizontal Retrace End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 05h
Default: 00h

D7 Horizontal Blank End Bit[5]
D[6:5] Horizontal Retrace Delay Bit[1:0]
00: Skew 0 character clock
01: Skew 1 character clock
10: Skew 2 character clocks
11: Skew 3 character clocks

D[4:0] Horizontal Retrace End Bit[4:0]

**6.2.8 CR6: Vertical Total**

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 06h
Default: 00h
D[7:0] Vertical Total Bit[7:0]

6.2.9 CR7: Overflow Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 07h
Default: 00h
D7 Vertical Retrace Start Bit[9]
D6 Vertical Display Enable End Bit[9]
D5 Vertical Total Bit[9]
D4 Line Compare Bit[8]
D3 Vertical Blank Start Bit[8]
D2 Vertical Retrace Start Bit[8]
D1 Vertical Display Enable End Bit[8]
D0 Vertical Total Bit[8]

6.2.10 CR8: Preset Row Scan

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 08h
Default: 00h
D7 Reserved
D[6:5] Byte Panning Control Bit[1:0]
D[4:0] Preset Row Scan Bit[4:0]

6.2.11 CR9: Maximum Scan Line/Text Character Height

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 09h
Default: 00h
D7 Double Scan
0: Disable
1: Enable 400 lines display
D6 Line Compare Bit[9]
D5 Vertical Blank Start Bit[9]
D[4:0] Character Cell Height Bit[4:0]

6.2.12 CRA: Text Cursor Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ah
Default: 00h
D[7:6] Reserved
D5 Text Cursor Off
0: Text Cursor On
1: Text Cursor Off
D[4:0] Text Cursor Start Bit[4:0]

**6.2.13 CRB: Text Cursor End**

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Bh
Default: 00h

D7 Reserved
D[6:5] Text Cursor Skew
00: No skew
01: Skew one character clock
10: Skew two character clocks
11: Skew three character clocks
D[4:0] Text Cursor End Bit[4:0]

6.2.14 CRC: Screen Start Address High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Ch
Default: 00h
D[7:0] Screen Start Address Bit[15:8]

6.2.15 CRD: Screen Start Address Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Dh
Default: 00h
D[7:0] Screen Start Address Bit[7:0]

6.2.16 CRE: Text Cursor Location High

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Eh
Default: 00h
D[7:0] Text Cursor Location Bit[15:8]

6.2.17 CRF: Text Cursor Location Low

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 0Fh
Default: 00h
D[7:0] Text Cursor Location Bit[7:0]

6.2.18 CR10: Vertical Retrace Start

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 10h
Default: 00h
D[7:0] Vertical Retrace Start Bit[7:0]

**6.2.19 CR11: Vertical Retrace End**

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 11h
Default: 00h

D7 Write Protect for CR0 to CR7
0: Disable Write Protect
1: Enable Write Protect

D6 Alternate Refresh Rate
0: Selects three refresh cycles per scanline
1: Selects five refresh cycles per scanline

D5 Vertical Interrupt Enable
0: Enable
1: Disable

D4 Vertical Interrupt Clear
0: Clear
1: Not Clear

D[3:0] Vertical Retrace End Bit[3:0]

6.2.20 CR12: Vertical Display Enable End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 12h
Default: 00h

D[7:0] Vertical Display Enable End Bit[7:0]

6.2.21 CR13: Screen Offset

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 13h
Default: 00h

D[7:0] Screen Offset Bit[7:0]

6.2.22 CR14: Underline Location Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 14h
Default: 00h

D7 Reserved

D6 Doubleword Mode Enable
0: Disable
1: Enable

D5 Count by 4
0: Disable
1: Enable

D[4:0] Underline Location Bit[4:0]

**6.2.23 CR15: Vertical Blank Start**

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 15h
Default: 00h
D[7:0] Vertical Blank Start Bit[7:0]

6.2.24 CR16: Vertical Blank End

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 16h
Default: 00h
D[7:0] Vertical Blank End Bit[7:0]

6.2.25 CR17: Mode Control Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 17h
Default: 00h

| | |
|----|---|
| D7 | Hardware Reset 0: Disable horizontal and vertical retrace outputs 1: Enable horizontal and vertical retrace outputs |
| D6 | Word/Byte Address Mode 0: Set the memory address mode to word 1: Set the memory address mode to byte |
| D5 | Address Wrap 0: Disable the full 256K of memory 1: Enable the full 256K of memory |
| D4 | Reserved |
| D3 | Count by Two 0: Byte refresh 1: Word refresh |
| D2 | Horizontal Retrace Select 0: Normal 1: Double Scan |
| D1 | RA1 replace MA14 0: Enable 1: Disable |
| D0 | RA0 replace MA13 0: Enable 1: Disable |

6.2.26 CR18: Line Compare Register

Register Type: Read/Write
Read/Write Port: 3B5/3D5, Index 18h
Default: 00h
D[7:0] Line Compare Bit[7:0]

**6.2.27 CR19: Extended Signature Read-Back Register 0**

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 19h
Default: 00h
D[7:0] Signature read-back bit[7:0]

6.2.28 CR1A: Extended Signature Read-Back Register 1

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 1Ah
Default: 00h
D[7:0] Signature read-back bit[15:8]

6.2.29 CR22: Graphics Data Latch Readback Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 22h
D[7:0] Graphics Data Latch bit[7:0]

6.2.30 CR24: Attribute Controller Toggle Readback Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 24h
D7 Attribute Controller Toggle
D[6:0] Reserved

6.2.31 CR26: Attribute Controller Index Readback Register

Register Type: Read Only
Read/Write Port: 3B5/3D5, Index 26h
D[7:6] Reserved
D5 Video Enable
D[4:0] Attribute Controller Index bit[8:4]



6.3 Sequencer Registers

6.3.1 Sequencer Index Register

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Sequencer Index Bit[5:0]

Table of Sequencer Registers

| Index (3C4) | Sequencer Register (3C5) |
|-------------|----------------------------|
| 00 | Reset Register |
| 01 | Clock Mode |
| 02 | Color Plane Write Enable |
| 03 | Character Generator Select |
| 04 | Memory Mode |

6.3.2 SR0: Reset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 00h
Default: 00h
D[7:2] Reserved
D1 Synchronous reset
0: Reset
1: Normal
D0 Asynchronous reset
0: Reset
1: Normal

6.3.3 SR1: Clock Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 01h
Default: 00h
D[7:6] Reserved
D5 Screen Off
0: Display On
1: Display Off
D4 Shifter Load 32 enable
0: Disable
1: Data shifter loaded every 4th Character Clock



| | |
|----|---|
| D3 | Dot Clock Divide by 2 enable 0: Disable 1: Video Clock is divided by 2 to generate Dot Clock |
| D2 | Shifter Load 16 (while D4=0) 0: Disable 1: Data shifter loaded every 2nd Character Clock |
| D1 | Reserved |
| D0 | 8/9 Dot Clock 0: Dot Clock is divided by 9 to generate Character Clock 1: Dot Clock is divided by 8 to generate Character Clock |

6.3.4 SR2: Color Plane Write Enable Register

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 02h |
| Default: | 00h |
| D[7:4] | Reserved |
| D3 | Plane 3 write enable 0: Disable 1: Enable |
| D2 | Plane 2 write enable 0: Disable 1: Enable |
| D1 | Plane 1 write enable 0: Disable 1: Enable |
| D0 | Plane 0 write enable 0: Disable 1: Enable |

6.3.5 SR3: Character Generator Select Register

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 03h |
| Default: | 00h |
| D[7:6] | Reserved |
| D5 | Character generator table B select Bit[2] |
| D4 | Character generator table A select Bit[2] |
| D[3:2] | Character generator table B select Bit[1:0] |
| D[1:0] | Character generator table A select Bit[1:0] |

**Table 6-1 Table of Selecting Active Character Generator**

| D5 | D3 | D2 | Used when text attribute bit 3 is 1 |
|----|----|----|-------------------------------------|
| D4 | D1 | D0 | Used when text attribute bit 3 is 0 |
| 0 | 0 | 0 | Character Table 1 |
| 0 | 0 | 1 | Character Table 2 |
| 0 | 1 | 0 | Character Table 3 |
| 0 | 1 | 1 | Character Table 4 |
| 1 | 0 | 0 | Character Table 5 (VGA only) |
| 1 | 0 | 1 | Character Table 6 (VGA only) |
| 1 | 1 | 0 | Character Table 7 (VGA only) |
| 1 | 1 | 1 | Character Table 8 (VGA only) |

6.3.6 SR4: Memory Mode Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 04h
Default: 00h

D[7:4] Reserved
D3 Chain-4 Mode enable
0: Disable
1: Enable
D2 Odd/Even Mode enable
0: Enable
1: Disable
D1 Extended Memory
0: Select 64K
1: Select 256K
D0 Reserved



6.4 Graphics Controller Registers

6.4.1 Graphics Controller Index Register

Register Type: Read/Write
 Read/Write Port: 3CE
 Default: 00h
 D[7:4] Reserved
 D[3:0] Graphics Controller Index Bit[3:0]

| Index (3CE) | Graphics Controller Register (3CF) |
|-------------|------------------------------------|
| 00 | Set/Reset Register |
| 01 | Set/Reset Enable Register |
| 02 | Color Compare Register |
| 03 | Data Rotate & Function Select |
| 04 | Read Plane Select Register |
| 05 | Mode Register |
| 06 | Miscellaneous Register |
| 07 | Color Don't Care Register |
| 08 | Bit Mask Register |

6.4.2 GR0: Set/Reset Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 00h
 Default: 00h
 D[7:4] Reserved
 D3 Set/Reset Map for plane 3
 D2 Set/Reset Map for plane 2
 D1 Set/Reset Map for plane 1
 D0 Set/Reset Map for plane 0

6.4.3 GR1: Set/Reset Enable Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 01h
 Default: 00h
 D[7:4] Reserved
 D3 Enable Set/Reset for plane 3
 0: Disable
 1: Enable
 D2 Enable Set/Reset for plane 2
 0: Disable
 1: Enable
 D1 Enable Set/Reset for plane 1
 0: Disable
 1: Enable
 D0 Enable Set/Reset for plane 0



0: Disable

1: Enable

6.4.4 GR2: Color Compare Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 02h
 Default: 00h

D[7:4] Reserved
 D3 Color Compare Map for plane 3
 D2 Color Compare Map for plane 2
 D1 Color Compare Map for plane 1
 D0 Color Compare Map for plane 0

6.4.5 GR3: Data Rotate/Function Select Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 03h
 Default: 00h

D[7:5] Reserved
 D[4:3] Function Select

Table of Function Select

| D4 | D3 | Function |
|----|----|----------------------------------|
| 0 | 0 | write data unmodified |
| 0 | 1 | write data AND processor latches |
| 1 | 0 | write data OR processor latches |
| 1 | 1 | write data XOR processor latches |

D[2:0] Rotate Count

Table of Rotate Count

| D2 | D1 | D0 | Right Rotation |
|----|----|----|----------------|
| 0 | 0 | 0 | none |
| 0 | 0 | 1 | 1 bits |
| 0 | 1 | 0 | 2 bits |
| 0 | 1 | 1 | 3 bits |
| 1 | 0 | 0 | 4 bits |
| 1 | 0 | 1 | 5 bits |
| 1 | 1 | 0 | 6 bits |
| 1 | 1 | 1 | 7 bits |

6.4.6 GR4: Read Plane Select Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 04h
 Default: 00h



D[7:2] Reserved
 D[1:0] Read Plane Select bit 1, 0
 00: Plane 0
 01: Plane 1
 10: Plane 2
 11: Plane 3

6.4.7 GR5: Mode Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 05h
 Default: 00h

D7 Reserved
 D6 256-color Mode
 0: Disable
 1: Enable
 D5 Shift Register Mode
 0: Configure shift register to be EGA compatible
 1: Configure shift register to be CGA compatible
 D4 Odd/Even Addressing Mode enable
 0: Disable
 1: Enable
 D3 Read Mode
 0: Map Select Read
 1: Color Compare Read
 D2 Reserved
 D[1:0] Write mode

Table for Write Mode

| D1 | D0 | Mode Selected |
|----|----|--|
| 0 | 0 | <i>Write Mode 0: Direct processor write (Data Rotate, Set/Reset may apply).</i> |
| 0 | 1 | <i>Write Mode 1: Use content of latches as write data.</i> |
| 1 | 0 | <i>Write Mode 2: Color Plane n(0-3) is filled with the value of bit m in the processor write data.</i> |
| 1 | 1 | <i>Write Mode 3: Color Plane n(0-3) is filled with 8 bits of the color value contained in the Set/Reset Register for that plane. The Enable Set/Reset Register is not effective. Processor data will be AND with Bit Mask Register content to form new bit mask pattern. (data rotate may apply)</i> |

**6.4.8 GR6: Miscellaneous Register**

Register Type: Read/Write
 Read/Write Port: 3CF, Index 06h
 Default: 00h

D[7:4] Reserved
 D[3:2] Memory Address Select

Table of Memory Address Select

| D3 | D2 | Address range |
|----|----|----------------|
| 0 | 0 | A0000 to BFFFF |
| 0 | 1 | A0000 to AFFFF |
| 1 | 0 | B0000 to B7FFF |
| 1 | 1 | B8000 to BFFFF |

D1 Chain Odd And Even Maps
 0: Disable
 1: Enable
 D0 Graphics Mode Enable
 0: Select alphanumeric mode
 1: Select graphics mode

6.4.9 GR7: Color Don't Care Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 07h
 Default: 00h

D[7:4] Reserved
 D3 Plane 3 Don't Care
 0: Disable color comparison
 1: Enable color comparison
 D2 Plane 2 Don't Care
 0: Disable color comparison
 1: Enable color comparison
 D1 Plane 1 Don't Care
 0: Disable color comparison
 1: Enable color comparison
 D0 Plane 0 Don't Care
 0: Disable color comparison
 1: Enable color comparison

6.4.10 GR8: Bit Mask Register

Register Type: Read/Write
 Read/Write Port: 3CF, Index 08h
 Default: 00h

D[7:0] Bit Mask Enable Bit[7:0]



6.5 Attribute Controller and Video DAC Registers

6.5.1 Attribute Controller Index Register

Register Type: Read/Write
Read Port: 3C0
Write Port: 3C0
Default: 00h

D[7:6] Reserved
D5 Palette Address Source
0: From CPU
1: From CRT
D[4:0] Attribute Controller Index Bit[4:0] (00h-14h)

| Index (3C0) | Attribute Controller Register (3C0) |
|-------------|-------------------------------------|
| 00h | Color Palette Register 0 |
| 01h | Color Palette Register 1 |
| 02h | Color Palette Register 2 |
| 03h | Color Palette Register 3 |
| 04h | Color Palette Register 4 |
| 05h | Color Palette Register 5 |
| 06h | Color Palette Register 6 |
| 07h | Color Palette Register 7 |
| 08h | Color Palette Register 8 |
| 09h | Color Palette Register 9 |
| 0Ah | Color Palette Register 10 |
| 0Bh | Color Palette Register 11 |
| 0Ch | Color Palette Register 12 |
| 0Dh | Color Palette Register 13 |
| 0Eh | Color Palette Register 14 |
| 0Fh | Color Palette Register 15 |
| 10h | Mode Control Register |
| 11h | Screen Border Color |
| 12h | Color Plane Enable Register |
| 13h | Pixel Panning Register |
| 14h | Color Select Register (VGA) |

**6.5.2 AR0~ARF: Palette Registers**

| | |
|----------------|----------------------|
| Register Type: | Read/Write |
| Read Port: | 3C1, Index 00h ~ 0Fh |
| Write Port: | 3C0, Index 00h ~ 0Fh |
| Default: | 00h |
| D[7:6] | Reserved |
| D[5:0] | Palette Entries |

6.5.3 AR10: Mode Control Register

| | |
|----------------|---|
| Register Type: | Read/Write |
| Read Port: | 3C1, Index 10h |
| Write Port: | 3C0, Index 10h |
| Default: | 00h |
| D7 | P4, P5 Source Select 0: AR0-F Bit[5:4] are used as the source for the Lookup Table Address Bit[5:4] 1: AR14 Bit[1:0] are used as the source for the Lookup Table Address Bit[5:4] |
| D6 | Pixel Double Clock Select 0: The pixels are clocked at every clock cycle 1: The pixels are clocked at every other clock cycle |
| D5 | PEL Panning Compatibility with Line Compare 0: Disable 1: Enable |
| D4 | Reserved |
| D3 | Background Intensity or Blink enable (while the Character Attribute D7=1) 0: Background Intensity attribute enable 1: Background Blink attribute enable |
| D2 | Line Graphics enable 0: The ninth bit of nine-bit-wide character cell will be the same as the background. 1: The ninth bit of nine-bit-wide character cell will be made be the same as the eighth bit for character codes in the range C0h through DFh. |
| D1 | Display Type 0: The contents of the Attribute byte are treated as color attribute. 1: The contents of the Attribute byte are treated as MDA-compatible attribute. |
| D0 | Graphics/Text Mode 0: The Attribute Controller will function in text mode. 1: The Attribute Controller will function in graphics mode. |

**6.5.4 AR11: Screen Border Color**

Register Type: Read/Write
 Read Port: 3C1, Index 11h
 Write Port: 3C0, Index 11h
 Default: 00h
 D[7:6] Reserved
 D[5:0] Palette Entry

6.5.5 AR12: Color Plane Enable Register

Register Type: Read/Write
 Read Port: 3C1, Index 12h
 Write Port: 3C0, Index 12h
 Default: 00h
 D[7:6] Reserved
 D[5:4] Display Status MUX Bit[1:0]

These bits select two of the eight bits color outputs to be available in the status register. The output color combinations available on the status bits are as follows:

Table for Video Read-back Through Diagnostic Bit (I)

| Color Plane Enable Register | | Input Status Register 1 (Refer to 6.1.3 on page 48) | |
|-----------------------------|----|---|-----------------|
| D5 | D4 | D5 | D4 |
| 0 | 0 | Red | Blue |
| 0 | 1 | Secondary Red | Secondary Green |
| 1 | 0 | Secondary Blue | Green |
| 1 | 1 | Unused | Unused |

Table for Video Read-back Through Diagnostic Bit (II)

| Color Plane Enable Register | | Input Status Register 1 (Refer to 6.1.3 on page 48) | |
|-----------------------------|----|---|----|
| D5 | D4 | D5 | D4 |
| 0 | 0 | P2 | P0 |
| 0 | 1 | P5 | P4 |
| 1 | 0 | P3 | P1 |
| 1 | 1 | P7 | P6 |

D[3:0] Enable Color Plane Bit[3:0]

6.5.6 AR13: Pixel Panning Register

Register Type: Read/Write
 Read Port: 3C1, Index 13h
 Write Port: 3C0, Index 13h
 Default: 00h
 D[7:4] Reserved
 D[3:0] Pixel Pan Bit[3:0]

This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:



| D3 | D2 | D1 | D0 | Monochrome Text | VGA Mode 13 | All others |
|----|----|----|----|-----------------|-------------|------------|
| 0 | 0 | 0 | 0 | 8 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | Invalid | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 2 |
| 0 | 0 | 1 | 1 | 2 | Invalid | 3 |
| 0 | 1 | 0 | 0 | 3 | 2 | 4 |
| 0 | 1 | 0 | 1 | 4 | Invalid | 5 |
| 0 | 1 | 1 | 0 | 5 | 3 | 6 |
| 0 | 1 | 1 | 1 | 6 | Invalid | 7 |
| 1 | 0 | 0 | 0 | 7 | Invalid | Invalid |
| 1 | 0 | 0 | 1 | Invalid | Invalid | Invalid |
| 1 | 0 | 1 | 0 | Invalid | Invalid | Invalid |
| 1 | 0 | 1 | 1 | Invalid | Invalid | Invalid |
| 1 | 1 | 0 | 0 | Invalid | Invalid | Invalid |
| 1 | 1 | 0 | 1 | Invalid | Invalid | Invalid |
| 1 | 1 | 1 | 0 | Invalid | Invalid | Invalid |
| 1 | 1 | 1 | 1 | Invalid | Invalid | Invalid |

6.5.7 AR14: Color Select Register

Register Type: Read/Write

Read Port: 3C1, Index 14h

Write Port: 3C0, Index 14h

Default: 00h

D[7:4] Reserved

D[3:2] Color Bit[7:6]

These two bits are concatenated with the six bits from the Palette Register to form the address into the LUT and to drive P[7:6]

D[1:0] Color Bit[5:4]

If AR10 D7 is programmed to a '1', these two bits replace the corresponding two bits from the Palette Register to form the address into the LUT and to drive P[5:4]. If AR10 D7 is programmed to a '0', these two bits are ignored.



6.6 Color Registers

6.6.1 DAC Status Register

| | |
|----------------|---------------------------------|
| Register Type: | Read Only |
| Read Port: | 3C7 |
| Default: | 00h |
| D[7:2] | Reserved |
| D[1:0] | DAC State Bit[1:0] |
| | 00: Write Operation in progress |
| | 11: Read Operation in progress |

6.6.2 DAC Index Register (Read Mode)

| | |
|----------------|--------------------|
| Register Type: | Write Only |
| Write Port: | 3C7 |
| Default: | 00h |
| D[7:0] | DAC Index Bit[7:0] |

6.6.3 DAC Index Register (Write Mode)

| | |
|------------------|--------------------|
| Register Type: | Read/Write |
| Read/Write Port: | 3C8 |
| Default: | 00h |
| D[7:0] | DAC Index Bit[7:0] |

6.6.4 DAC Data Register

| | |
|------------------|----------------|
| Register Type: | Read/Write |
| Read/Write Port: | 3C9 |
| Default: | 00h |
| D[7:6] | Reserved |
| D[5:0] | DAC Data [5:0] |

Before writing to this register, 3C8h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue values for the DAC entry are written. After the third value is written, the values are transferred to the LUT and the DAC index is incremented in case new values for the next DAC index are to be written.

Before reading from this register, 3C7h is written with the DAC index. Then three values, corresponding to the Red, Green, and Blue value for the DAC entry may be read from this DAC index. After the third value is read, the DAC index is incremented in case the value for the next DAC index to be read.

6.6.5 PEL Mask Register

| | |
|------------------|---------------------|
| Register Type: | Read/Write |
| Read/Write Port: | 3C6 |
| Default: | 00h |
| D[7:0] | Pixel Mask Bit[7:0] |

This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.



6.7 SiS 6205 Extended Registers

6.7.1 Extended Index Register

Register Type: Read/Write
Read/Write Port: 3C4
Default: 00h
D[7:6] Reserved
D[5:0] Extended Register Index Bit[5:0] (05h ~ 37h)

| Index (3C4) | Extended Enhanced Register (3C5) |
|-------------|--|
| 05h | Extended Password/Identification Register |
| 06h | Extended Graphics Mode Control Register |
| 07h | Extended Misc. Control Register 0 |
| 08h | Extended CRT/CPU Threshold Control Register 0 |
| 09h | Extended CRT/CPU Threshold Control Register 1 |
| 0Ah | Extended CRT Overflow Register |
| 0Bh | Extended Misc. Control Register 1 |
| 0Ch | Extended Misc. Control Register 2 |
| 0Dh | Extended Configuration Status 0 |
| 0Eh | Extended Configuration Status 1 |
| 0Fh | Extended Scratch Register 0 |
| 10h | Extended Scratch Register 1 |
| 11h | Extended DDC and Power Control Register |
| 14h | Extended Hardware Cursor Color 0 Red Register |
| 15h | Extended Hardware Cursor Color 0 Green Register |
| 16h | Extended Hardware Cursor Color 0 Blue Register |
| 17h | Extended Hardware Cursor Color 1 Red Register |
| 18h | Extended Hardware Cursor Color 1 Green Register |
| 19h | Extended Hardware Cursor Color 1 Blue Register |
| 1Ah | Extended Hardware Cursor Horizontal Start Register 0 |
| 1Bh | Extended Hardware Cursor Horizontal Start Register 1 |
| 1Ch | Extended Hardware Cursor Horizontal Preset Register |
| 1Dh | Extended Hardware Cursor Vertical Start Register 0 |
| 1Eh | Extended Hardware Cursor Vertical Start Register 1 |
| 1Fh | Extended Hardware Cursor Vertical Preset Register |
| 20h | Extended Linear Addressing Base Address Register 0 |
| 21h | Extended Linear Addressing Base Address Register 1 |
| 22h | Extended Standby/Suspend Timer Register |
| 23h | Extended Misc. Control Register 3 |
| 24h | Extended Graphics Frame Buffer Location Address Register |
| 25h | Extended Scratch Register 2 |
| 26h | Extended Graphics Engine Register 0 |
| 27h | Extended Graphics Engine Register 1 |
| 28h | Extended Internal Memory Clock Register 0 |
| 29h | Extended Internal Memory Clock Register 1 |



| | |
|-----|--|
| 2Ah | Extended Internal Video Clock Register 0 |
| 2Bh | Extended Internal Video Clock Register 1 |
| 2Ch | Extended Turbo Queue Base Address |
| 2Dh | Extended Memory Start Control Register |
| 2Eh | Extended Shared Memory Control Register |
| 2Fh | Extended DRAM Frame Buffer Size Register |
| 30h | Extended Reserved Register |
| 31h | Extended Reserved Register |
| 32h | Extended Reserved Register |
| 33h | Extended Reserved Register |
| 34h | Extended Reserved Register |
| 35h | Extended Reserved Register |
| 36h | Extended Scratch Register 3 |
| 37h | Extended Scratch Register 4 |

6.7.2 SR5: Extended Password/Identification Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 05h

Default: 00h

D[7:0] Password/Identification Bit[7:0]

If 86h is written into this register, then A1h will be read from this register , and unlock all the extension registers.

If the value other than 86h is written into this register, then 21h will be read from this register, and lock all the extension registers.

6.7.3 SR6: Extended Graphics Mode Control Register

Register Type: Read/Write

Read/Write Port: 3C5, Index 06h

Default: 00h

D7 Graphics mode linear addressing enable

0: Disable

1: Enable

D6 Graphics mode hardware cursor display enable

0: Disable

1: Enable

D5 Graphics mode interlaced enable

0: Disable

1: Enable

D4 True-Color graphics mode enable

0: Disable

1: Enable

D3 64K-Color graphics mode enable

0: Disable

1: Enable

D2 32K-Color graphics mode enable

0: Disable



| | |
|----|-------------------------------|
| | 1: Enable |
| D1 | Enhanced graphics mode enable |
| | 0: Disable |
| | 1: Enable |
| D0 | Enhanced text mode enable |
| | 0: Disable |
| | 1: Enable |

6.7.4 SR7: Extended Misc. Control Register 0

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 07h |
| Default: | 00h |
| D7 | Intelligent CRT prefetch |
| | 0: Disable |
| | 1: Enable |
| D6 | Enable feature connector (VIDEO 0-7, PCLK) output |
| | 0: Enable |
| | 1: Disable |
| D5 | Internal RAMDAC operation |
| | 0: Low Speed mode (low power consumption) |
| | 1: High Speed mode |
| D4 | Extended video clock frequency divided by 2 |
| | 0: Disable |
| | 1: Enable |
| D[3:0] | Reserved |

6.7.5 SR8: Extended CRT/CPU Threshold Control Register 0

| | |
|------------------|--|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 08h |
| Default: | 00h |
| D[7:4] | CRT/CPU Arbitration Threshold Low Bit[3:0] |
| D[3:0] | CRT/Engine Threshold High Bit[3:0] |

6.7.6 SR9: Extended CRT/CPU Threshold Control Register 1

| | |
|------------------|------------------------------------|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 09h |
| Default: | 00h |
| D[7:4] | ASCII/Attribute Threshold Bit[3:0] |
| D[3:0] | CRT/CPU Threshold High Bit[3:0] |

6.7.7 SRA: Extended CRT Overflow Register

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 0Ah |
| Default: | 00h |
| D[7:4] | Extended Screen Offset Bit[11:8] |
| D3 | Extended Vertical Retrace Start Bit[10] |
| D2 | Extended Vertical Blank Start Bit[10] |



D1 Extended Vertical Display Enable End Bit[10]
D0 Extended Vertical Total Bit[10]

6.7.8 SRB: Extended Misc. Control Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Bh
Default: 00h

D7 True-Color Graphics mode RGB Sequence Selection
0: Red, Green, and Blue in byte order
1: Blue, Green, and Red in byte order

D[6:5] Memory-mapped I/O Space Selection Bit[1:0]
00: Disable
01: Select Axxxxh as Memory-mapped I/O Space
10: Select Bxxxxh as Memory-mapped I/O Space
11: Select PCI config register 14H as Memory-mapped I/O space

D4 True-Color frame rate modulation enable
0: Disable
1: Enable

D3 Dual segment register mode enable
0: Disable
1: Enable

D2 I/O gating enable while write-buffer is not empty
0: Disable
1: Enable

D1 16-color packed pixel enable
0: Disable
1: Enable

D0 CPU-driven BITBLT operation enable
0: Disable
1: Enable

6.7.9 SRC: Extended Misc. Control Register 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Ch
Default: 00h

D7 Graphics mode 32-bit memory access enable
0: Disable
1: Enable

D6 Text mode 16-bit memory access enable
0: Disable
1: Enable

D5 Read-ahead cache operation enable
0: Disable
1: Enable

D4 Reserved

D3 Test mode enable
0: Disable



| | |
|--------|---|
| | 1: Enable |
| D[2:1] | Memory Configuration Bit[1:0] |
| | 00: 1MByte/1 bank |
| | 01: 2MByte/2 banks |
| | 10: 4MByte/2 banks or 4 banks |
| | 11: 1MByte/2 banks |
| D0 | Synchronous reset timing generator enable |
| | 0: Disable |
| | 1: Enable |

6.7.10 SRD: Extended Configuration Status 0

| | |
|----------------|---|
| Register Type: | Read Only |
| Read Port: | 3C5, Index 0Dh |
| Default: | 00h |
| D7 | Enable 64K ROM decoding |
| | 0: Disable |
| | 1: Enable when MD23 is pulled up with resistor. |
| D6 | Clock Generator Selection |
| | 0: Select external clock generator (used for SiS internal test only) |
| | 1: Select internal clock generator when MD22 is pulled up with resistor |
| D5 | EDO DRAM Type Selection |
| | 0: Select Fast Page DRAM type |
| | 1: Select EDO DRAM type when MD21 is pulled up with resistor. |
| D4 | PCI Function Device Behavior |
| | 0: Single Function Device |
| | 1: Multi-Function Device when MD20 is pulled up with resistor. |
| D3 | 256Kx16 DRAM Type Selection |
| | 0: 1-WE/2-CAS 256Kx16 DRAM type |
| | 1: 2-WE/1-CAS 256Kx16 DRAM type when MD19 is pulled up with resistor. |
| D2 | BIOS ROM decoding logic |
| | 0: Enable |
| | 1: Disable when MD18 is pulled up with resistor. |
| D1 | Video subsystem enable/disable at power-on is |
| | 0: Controlled by System BIOS |
| | 1: Forced to disable when MD17 is pulled up with resistor. |
| D0 | Select I/O address 3C3h or 46E8h as video subsystem port |
| | 0: Select 3C3h |
| | 1: Select 46E8h when MD16 is pulled up with resistor. |

6.7.11 SRE: Extended Configuration Status 1

| | |
|----------------|-------------------|
| Register Type: | Read Only |
| Read Port: | 3C5, Index 0Eh |
| Default: | 00h |
| D[7:6] | Reserved |
| D5 | GPIO pin polarity |
| | 0: Positive |



| | |
|--------|---|
| D4 | 1: Negative when MD29 is pulled up with resistor. Enable VMI Interface 0: Disable |
| D3 | 1: Enable when MD28 is pulled up with resistor. INTA# Selection 0: Disable |
| D[2:0] | 1: Enable when MD27 is pulled up with resistor PCI Function Number Bit[2:0] which are configured by whether MD[26:24] are pulled up with resistors (bit=1) or not (bit=0) [000:111]=PCI Function Device Number[0:7] (default=0) |

6.7.12 SRF: Extended Scratch Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 0Fh
Default: 00h

D[7:0] Reserved for video BIOS

6.7.13 SR10: Extended Scratch Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 10h
Default: 00h

D[7:0] Reserved for video BIOS

6.7.14 SR11: Extended DDC and Power Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 11h
Default: 00h

| | |
|--------|--|
| D7 | Force VGA into suspend mode 0: Disable 1: Enable |
| D6 | Force VGA into standby mode 0: Disable 1: Enable |
| D5 | Enable video memory access as activation source 0: Disable 1: Enable |
| D4 | Enable keyboard and hardware cursor as system activation source 0: Disable 1: Enable |
| D[3:2] | Reserved |
| D1 | DDC DATA Programming While writing this bit, 0: Output '0' logic into DDC Data Signal. 1: Output '1' logic into DDC Data Signal. While reading this bit, 0: Get '0' logic from DDC Data Signal . 1: Get '1' logic from DDC Data Signal . |



D0 DDC CLK Programming
While writing this bit,
0: Output '0' logic into DDC Clock Signal.
1: Output '1' logic into DDC Clock Signal.
While reading this bit,
0: Get '0' logic from DDC Clock Signal .
1: Get '1' logic from DDC Clock Signal .

6.7.15 SR14: Extended Hardware Cursor Color 0 Red Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 14h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Red Bit[5:0]

6.7.16 SR15: Extended Hardware Cursor Color 0 Green Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 15h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Green Bit[5:0]

6.7.17 SR16: Extended Hardware Cursor Color 0 Blue Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 16h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 0 Blue Bit[5:0]

6.7.18 SR17: Extended Hardware Cursor Color 1 Red Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 17h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Red Bit[5:0]

6.7.19 SR18: Extended Hardware Cursor Color 1 Green Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 18h
Default: 00h

D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Green Bit[5:0]

6.7.20 SR19: Extended Hardware Cursor Color 1 Blue Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 19h



Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Color 1 Blue Bit[5:0]

6.7.21 SR1A: Extended Hardware Cursor Horizontal Start Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ah
Default: 00h
D[7:0] Hardware Cursor Horizontal Start Bit[7:0]

6.7.22 SR1B: Extended Hardware Cursor Horizontal Start Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Bh
Default: 00h
D[7:3] Reserved
D[2:0] Hardware Cursor Horizontal Start Bit[10:8]

6.7.23 SR1C: Extended Hardware Cursor Horizontal Preset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Ch
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Horizontal Preset Bit[5:0]

6.7.24 SR1D: Extended Hardware Cursor Vertical Start Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Dh
Default: 00h
D[7:0] Hardware Cursor Vertical Start Bit[7:0]

6.7.25 SR1E: Extended Hardware Cursor Vertical Start Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Eh
Default: 00h
D[7:4] Hardware Cursor Pattern Select Bit[3:0]
D3 Reserved
D[2:0] Hardware Cursor Vertical Start Bit[10:8]

6.7.26 SR1F: Extended Hardware Cursor Vertical Preset Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 1Fh
Default: 00h
D[7:6] Reserved
D[5:0] Hardware Cursor Vertical Preset Bit[5:0]

**6.7.27 SR20: Extended Linear Addressing Base Address Register 0**

Register Type: Read/Write
Read/Write Port: 3C5, Index 20h
Default: 00h

D[7:0] Linear Addressing Base Address Bit[26:19]

6.7.28 SR21: Extended Linear Addressing Base Address Register 1

Register Type: Read/Write
Read/Write Port: 3C5, Index 21h
Default: 00h

D7 Reserved
D[6:5] Linear Addressing Space Aperture Bit[1:0]
00: 512 KByte
01: 1 MByte
10: 2 Mbyte
11: 4MByte
D[4:0] Linear Addressing Base Address Bit[31:27]

6.7.29 SR22: Extended Standby/Suspend Timer Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 22h
Default: 00h

D[7:4] Suspend Timer Bit[3:0]
The resolution for Suspend Timer is 2 minutes.
D[3:0] Standby Timer Bit[3:0]
The resolution for Standby Timer is 2 minutes.

6.7.30 SR23: Extended Misc. Control Register 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 23h
Default: 00h

D7 General purpose output pin (GPIO)
When GPIO polarity is positive,
0: GPIO pin output low
1: GPIO pin output high
When GPIO polarity is negative,
0: GPIO pin output high
1: GPIO pin output low
D6 CRC Generator Enable
0: Disable
1: Enable
D5 EDO DRAM Enable Bit
0: Disable
1: Enable



| | |
|--------|---|
| D4 | Bypass SRAM 0: Disable 1: Enable |
| D3 | Video compatible Hardware Cursor visibility enable 0: Disable 1: Enable |
| D2 | Reserved |
| D[1:0] | DRAM Control Signal Delay Compensation Bit[1:0] 00: Delay 4 ns 01: Delay 5 ns 10: Delay 6 ns 11: Delay 7 ns |

6.7.31 SR24: Extended Graphics Frame Buffer Location Address Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 24h
Default: 00h

| | |
|--------|--|
| D[7:0] | Graphics Frame Buffer Location address Bits[7:0] When 32-bit mode, this register is in unit of 256 KB When 64-bit mode, this register is in unit of 512 KB |
|--------|--|

6.7.32 SR25: Extended Scratch Register 2

Register Type: Read/Write
Read/Write Port: 3C5, Index 25h
Default: 00h

| | |
|--------|-----------------------|
| D[7:0] | Reserved for VGA BIOS |
|--------|-----------------------|

6.7.33 SR26: Extended Graphics Engine Register 0

Register Type: Read/Write
Read/Write Port: 3C5, Index 26h
Default: 00h

| | |
|----|---|
| D7 | Enable ASCII Page-Hit Detection 0: Disable 1: Enable |
| D6 | Power-down Internal RAMDAC 0: Disable 1: Enable |
| D5 | PCI Burst-Write Mode enable 0: Disable 1: Enable |
| D4 | Continuous Memory Data Access Enable Bit 0: Disable 1: Enable |
| D3 | Internal VGAREQ* and VGAGNT* synchronize to HCLK 0: Asynchronous 1: Synchronous |
| D2 | Slow DRAM RAS pre-charge time |



| | |
|----|----------------------------------|
| | 0: Disable (3 MCLK/DRAM cycle) |
| | 1: Enable (4 MCLK/DRAM cycle) |
| D1 | Slow DRAM Timing enable |
| | 0: Disable (7 MCLK/DRAM cycle) |
| | 1: Enable (8 MCLK/DRAM cycle) |
| D0 | Swap CASA* and CASB* signal pins |
| | 0: Do not Swap |
| | 1: Swap |

6.7.34 SR27: Extended Graphics Engine Register 1

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 27h |
| Default: | 00h |
| D7 | Turbo Queue Engine enable |
| | 0: Disable |
| | 1: Enable |
| D6 | Graphics Engine Register Programming enable |
| | 0: Disable |
| | 1: Enable |
| D[5:4] | Logical Screen Width and Byte-Per-Pixel Select Bit[1:0] |
| | 00 1024, 256 colors or 512, 32k/64k colors |
| | 01 2048, 256 colors or 1024, 32k/64k colors |
| | 10 4096, 256 colors or 2048, 32k/64k colors |
| | 11 invalid |
| D[3:0] | Extended Screen Start Address Bit[19:16] |

6.7.35 SR28: Extended Internal Memory Clock Register 0

| | |
|------------------|-----------------------------|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 28h |
| Default: | 00h |
| D[7] | MCLK Divider |
| | 0: Do not divide |
| | 1: Divide by 2 |
| D[6:0] | MCLK Numerator Bit[6:0] |
| | [0000000:1111111] = [1:128] |

NOTE: For the operation of internal memory clock generation, please refer to "Sec.3.6 Internal Dual-Clock Synthesizer" on page 18.

6.7.36 SR29: Extended Internal Memory Clock Register 1

| | |
|------------------|--------------------------------------|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 29h |
| Default: | 00h |
| D7 | MCLK VCO Gain |
| | 0: Gain for low frequency operation |
| | 1: Gain for high frequency operation |
| D[6:5] | MCLK Post-Scale Bit[1:0] |
| | 00: Do not scale |



01: Scale by 2
10: Scale by 3
11: Scale by 4
D[4:0] MCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

NOTE: For the operation of internal memory clock generation, please refer to "Sec. 3.6 Internal Dual-Clock Synthesizer" on page 18.

6.7.37 SR2A: Extended Internal Video Clock Register 0

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Ah
Default: 00h

D[7] VCLK Divider
0: Do not divide
1: Divide by 2
D[6:0] VCLK Numerator Bit[6:0]
[0000000:1111111] = [1:128]

NOTE: For the operation of internal video clock generation, please refer to "Sec. 3.6 Internal Dual-Clock Synthesizer" on page 18.

6.7.38 SR2B: Extended Internal Video Clock Register 1

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Bh
Default: 00h

D7 VCLK VCO Gain
0: Gain for low frequency operation
1: Gain for high frequency operation
D[6:5] VCLK Post-Scale Bit[1:0]
00: Do not scale
01: Scale by 2
10: Scale by 3
11: Scale by 4
D[4:0] VCLK DeNumerator Bit[4:0]
[00000:11111] = [1:32]

NOTE: For the operation of internal video clock generation, please refer to "Sec. 3.6 Internal Dual-Clock Synthesizer" on page 18.

6.7.39 SR2C: Extended Turbo Queue Base Address

Register Type: Read/Write
Read/Write Port: 3C5h, Index 2Ch
Default: 00h

D7 Reserved
D[6:0] Turbo Queue Base Address Bit[6:0]

6.7.40 SR2D: Extended Memory Start Control Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 2Dh



| | |
|----------|---|
| Default: | 00h |
| D7 | Column Address Scramble Enable 0: Disable 1: Enable |
| D6 | Shared-memory 3-wire, 2-request Mode 0: Disable 1: Enable |
| D5 | Special Asymmetric DRAM Type 0: Disable 1: Enable |
| D4 | Shared-memory 2-wire, 2-request Mode 0: Disable 1: Enable |
| D[3:0] | Page Size Select 0000: 2 KB at 32-bit mode, 4 KB at 64-bit mode 0001: 4 KB at 32-bit mode, 8 KB at 64-bit mode 0010: 8 KB at 32-bit mode, 16 KB at 64-bit mode 0011: 16 KB at 32-bit mode, 32 KB at 64-bit mode 0100: 1 KB at 32-bit mode, 2 KB at 64-bit mode Others: Reserved |

6.7.41 SR2E: Extended Shared Memory Control Register

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5h, Index 2Eh |
| Default: | 00h |
| D[7:4] | Memory Address Scrambling Table Selection Bit[3:0] Refer to "Scrambling Table" on page 27. |
| D[3:2] | Row Address Selection Bit[1:0] 00: Row address [11:0] = memory address [20:9] 01: Row address [11:0] = memory address [21:10] 10: Row address [11:0] = memory address [22:11] 11: Row address [11:0] = memory address [23:12] |
| D[1:0] | RAS Selection Bit[1:0] 00: RAS0 active 01: RAS1 active 10: RAS2 active 11: RAS3 active |

6.7.42 SR2F: Extended DRAM Frame Buffer Size Register

| | |
|------------------|---|
| Register Type: | Read/Write |
| Read/Write Port: | 3C5, Index 2Fh |
| Default: | 00h |
| D7 | Read-Modified-Write Timing Selection 0: 5 MCLK 1: 6 MCLK |
| D6 | The High-Request Signal Polarity for shared-memory 3-wire, 2-request Mode |



| | |
|--------|---|
| | 0: Active low |
| | 1: Active high |
| D5 | Enable Fast Change Mode Timing |
| | 0: Disable |
| | 1: Enable |
| D4 | Enable Fast Page Flip |
| | 0: Disable |
| | 1: Enable |
| D3 | Enable Extend DRAM Frame Buffer Sizing |
| | 0: Disable |
| | 1: Enable |
| D[2:0] | Extended DRAM Frame Buffer Size Bit[2:0] |
| | 000: 256 KB for 32-bit DRAM data bus, 512 KB for 64-bit DRAM data bus |
| | 001: 512 KB for 32-bit DRAM data bus, 1 MB for 64-bit DRAM data bus |
| | 010: 768 KB for 32-bit DRAM data bus, 1.5 MB for 64-bit DRAM data bus |
| | 011: 1 MB for 32-bit DRAM data bus, 2 MB for 64-bit DRAM data bus |
| | 100: 1.25 MB for 32-bit DRAM data bus, 2.5 MB for 64-bit DRAM data bus |
| | 101: 1.5 MB for 32-bit DRAM data bus, 3 MB for 64-bit DRAM data bus |
| | 110: 1.75 MB for 32-bit DRAM data bus, 3.5 MB for 64-bit DRAM data bus |
| | 111: 2 MB for 32-bit DRAM data bus, 4 MB for 64-bit DRAM data bus |

6.7.43 SR30: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 30h
Default: 00h

D[7:0] Reserved

6.7.44 SR31: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 31h
Default: 00h

D[7:0] Reserved

6.7.45 SR32: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 32h
Default: 00h

D[7:0] Reserved



6.7.46 SR33: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 33h
Default: 00h
D[7:0] Reserved

6.7.47 SR34: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 34h
Default: 00h
D[7:0] Reserved

6.7.48 SR35: Extended Reserved Register

Register Type: Read/Write
Read/Write Port: 3C5, Index 35h
Default: 00h
D[7:0] Reserved

6.7.49 SR36: Extended Scratch Register 3

Register Type: Read/Write
Read/Write Port: 3C5, Index 36h
Default: 00h
D[7:0] Reserved for VGA BIOS

6.7.50 SR37: Extended Scratch Register 4

Register Type: Read/Write
Read/Write Port: 3C5, Index 37h
Default: 00h
D[7:0] Reserved for VGA BIOS



6.8 Graphics Engine Related Registers

SiS 6205 integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in SiS 6205 include BitBlt, BitBlt with mask, Color/Font Expansion, Enhanced Color/Font Expansion, Line Drawing, and Direct Draw.

Since the register formats for the line drawing and Direct Draw are different from those of the other general engine functions, we would like to describe these three register formats separately in the following paragraphs:

6.8.1 Register Format for General Engine Functions

6.8.2 Register Format for Line Drawing

6.8.3 Register Format for Direct Draw

6.8.1 Register Format for General Engine Functions

The following table shows the register format for the general Graphics Engine functions.

| D[31:24] | D[23:16] | D[15:08] | D[07:00] | I/O Address |
|--------------------|---------------------------------|----------------------|------------|-------------|
| Reserved | SRC Start Linear Address [21:0] | | | 8280h |
| Reserved | DST Start Linear Address [21:0] | | | 8284h |
| DST Pitch | | SRC Pitch | | 8288h |
| Rectangular Height | | Rectangular Width | | 828Ch |
| FG Rop | FG (Foreground) Color | | | 8290h |
| BG Rop | BG (Background) Color | | | 8294h |
| Mask3 | Mask2 | Mask1 | Mask0 | 8298h |
| Mask7 | Mask6 | Mask5 | Mask4 | 829Ch |
| Top Clipping | | Left Clipping | | 82A0h |
| Bottom Clipping | | Right Clipping | | 82A4h |
| Command 1 | Command 0 | Command Queue Status | | 82A8h |
| Pattern 3 | Pattern 2 | Pattern 1 | Pattern 0 | 82ACh |
| Pattern 7 | Pattern 6 | Pattern 5 | Pattern 4 | 82B0h |
| Pattern 11 | Pattern 10 | Pattern 9 | Pattern 8 | 82B4h |
| Pattern 15 | Pattern 14 | Pattern 13 | Pattern 12 | 82B8h |
| Pattern 19 | Pattern 18 | Pattern 17 | Pattern 16 | 82BCh |
| Pattern 23 | Pattern 22 | Pattern 21 | Pattern 20 | 82C0h |
| Pattern 27 | Pattern 26 | Pattern 25 | Pattern 24 | 82C4h |
| Pattern 31 | Pattern 30 | Pattern 29 | Pattern 28 | 82C8h |
| Pattern 35 | Pattern 34 | Pattern 33 | Pattern 32 | 82CCh |
| Pattern 39 | Pattern 38 | Pattern 37 | Pattern 36 | 82D0h |
| Pattern 43 | Pattern 42 | Pattern 41 | Pattern 40 | 82D4h |
| Pattern 47 | Pattern 46 | Pattern 45 | Pattern 44 | 82D8h |
| Pattern 51 | Pattern 50 | Pattern 49 | Pattern 48 | 82DCh |
| Pattern 55 | Pattern 54 | Pattern 53 | Pattern 52 | 82E0h |
| Pattern 59 | Pattern 58 | Pattern 57 | Pattern 56 | 82E4h |
| Pattern 63 | Pattern 62 | Pattern 61 | Pattern 60 | 82E8h |

**Source Start Linear Address**

Register Type: Read/Write
Read/Write Port: 8280h~8283h
Default: 00h
D[31:22] Reserved
D[21:0] Source Start Linear Address Bit[21:0]

Destination Start Linear Address

Register Type: Read/Write
Read/Write Port: 8284h~8287h
Default: 00h
D[31:22] Reserved
D[21:0] Destination Start Linear Address Bit[21:0]

Source Pitch

Register Type: Read/Write
Read/Write Port: 8288h~8289h
Default: 00h
D[15:12] Reserved
D[11:0] Source Pitch Bit[11:0]

Destination Pitch

Register Type: Read/Write
Read/Write Port: 828Ah~828Bh
Default: 00h
D[15:12] Reserved
D[11:0] Destination Pitch Bit[11:0]

Rectangular Width

Register Type: Read/Write
Read/Write Port: 828Ch~828Dh
Default: 00h
D[15:12] Reserved
D[11:0] Destination Rectangular Width Bit[11:0]

Rectangular Height

Register Type: Read/Write
Read/Write Port: 828Eh~828Fh
Default: 00h
D[15:12] Reserved
D[11:0] Destination Rectangular Height Bit[11:0]

Foreground Color

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h
D[23:0] Foreground Color Bit[23:0]

**FG Rop**

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

Background Color

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0] Background Color Bit[23:0]

BG Rop

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

Mono Mask Register

Register Type: Read/Write
Read/Write Port: 8298h~829Fh
Default: 00h

D[63:0] Mono Mask Bit[63:0]

Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h

D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h



Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read
Read/Write Port: 82A8h~82A9h
Default: 00h

If Hardware Command Queue is enable, then

D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] Head/Tail Index Bit[15:0]

The Head Index is written into this register, and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write
Read/Write Port: 82AAh
Default: 00h

D7 Rectangular clipping mode
0: Clipping internal region
1: Clipping external region
D6 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic
D5 Y direction control
0: Y counter decrease
1: Y counter increase
D4 X direction control
0: X counter decrease
1: X counter increase
D[3:2] Pattern select bit 1-0
00: From background color registers
01: From foreground color registers
10: From pattern registers
11: Reserved
D[1:0] Source select bit 1-0
00: From background color registers
01: From foreground color registers
10: From video memory
11: From CPU-driven BitBlt source data

Command Register 1

Register Type: Read/Write
Read/Write Port: 82ABh
Default: 00h

D7 Hardware Command Queue status



| | |
|--------|---|
| | 0: Hardware Command queue is not empty |
| | 1: Hardware Command queue is empty |
| D6 | Graphics engine status |
| | 0: Graphics engine is idle and Hardware command queue is empty |
| | 1: Graphics engine is busy or Hardware command queue is not empty |
| D5 | Enhanced Color/Font Expansion |
| | 0: Disable enhanced color expansion |
| | 1: Enable enhanced color expansion |
| D4 | Software Command Queue Status |
| | 0: Software Command queue empty |
| | 1: Software Command queue not empty |
| D3 | Line drawing last pixel control |
| | 0: Last pixel will be drawn |
| | 1: Last pixel will not be drawn |
| D2 | Line drawing major axial selection |
| | 0: Y-axial is major |
| | 1: X-axial is major |
| D[1:0] | Command type select Bit[1:0] |
| | 00: BitBlt |
| | 01: BitBlt with mask |
| | 10: Color/Font expansion |
| | 11: Line drawing |

NOTE: Word_Writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.

Pattern Register n

Register Type: Read/Write

Read/Write Port: 82ACh-82EBh

Default: 00h

D[7:0] For 256 color mode with BitBlt engine, these registers store the 8x8 color bitmap.
For Color-Expansion, these registers store the monochrome bitmap, thus it can expand 512 pixels at a time.



6.8.2 Register Format for Line Drawing

The register format for Line-Drawing is shown in following table.

| D[31:24] | D[23:16] | D[15:08] | D[07:00] | IO Address |
|-----------------|-----------------------|-------------------------|----------|------------|
| Reserved | | X Start | | 8280h |
| Reserved | | Y Start | | 8284h |
| Reserved | | Reserved | | 8288h |
| Reserved | | Major Axial Pixel Count | | 828Ch |
| FG Rop | FG (Foreground) Color | | | 8290h |
| BG Rop | BG (Background) Color | | | 8294h |
| K2 Term | | K1 Term | | 8298h |
| Line Style | | Error Term | | 829Ch |
| Top Clipping | | Left Clipping | | 82A0h |
| Bottom Clipping | | Right Clipping | | 82A4h |
| Command/Status | | Reserved | Status 0 | 82A8h |

X Start

Register Type: Read/Write
 Read/Write Port: 8280h~8281h
 Default: 00h

D[15:12] Reserved
 D[11:0] X Start Bit[11:0]

Y Start

Register Type: Read/Write
 Read/Write Port: 8284h~8285h
 Default: 00h

D[15:12] Reserved
 D[11:0] Y Start Bit[11:0]

Major Axial Pixel Count

Register Type: Read/Write
 Read/Write Port: 828Ch~828Dh
 Default: 00h

D[15:12] Reserved
 D[11:0] Major Axial Pixel Count Bit[11:0]

Foreground Color

Register Type: Read/Write
 Read/Write Port: 8290h~8292h
 Default: 00h

D[23:0] Foreground Color Bit[23:0]

**FG Rop**

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h

D[7:0] Foreground Raster Operation Bit[7:0]

Background Color

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h

D[23:0] Background Color Bit[23:0]

BG Rop

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h

D[7:0] Background Raster Operation Bit[7:0]

K1 Term

Register Type: Read/Write
Read/Write Port: 8298h~8299h
Default: 00h

D[15:14] Reserved
D[13:0] K1 Term Bit[13:0]

K2 Term

Register Type: Read/Write
Read/Write Port: 829Ah~829Bh
Default: 00h

D15:14] Reserved
D[13:0] K2 Term Bit[13:0]

Error Term

Register Type: Read/Write
Read/Write Port: 829Ch~829Dh
Default: 00h

D[15:14] Reserved
D[13:0] Error Term Bit[13:0]

Line Style

Register Type: Read/Write
Read/Write Port: 829Eh~829Fh
Default: 00h

D[15:0] Style Pattern Bit[15:0]

Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h



Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read/Write
Read/Write Port: 82A8h~82A9h
Default: 00h

If Hardware Command Queue is enable, then

D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] Head/Tail Index Bit[15:0]
The Head Index is written into this register, and the Tail Index is read from this registers.

Command Register 0

Register Type: Read/Write
Read/Write Port: 82AAh
Default: 00h
D7 Rectangular Clipping Mode
0: Clipping internal region
1: Clipping external region
D6 Rectangular Clipping Control
0: Disable rectangular clipping logic
1: Enable rectangular clipping logic



| | |
|--------|--|
| D5 | Y direction control 0: Y counter decrease 1: Y counter increase |
| D4 | X direction control 0: X counter decrease 1: X counter increase |
| D[3:2] | Pattern select bit 1-0 00: From background color registers 01: From foreground color registers 10: From pattern registers 11: Reserved |
| D[1:0] | Source select bit 1-0 00: From background color registers 01: From foreground color registers 10: From video memory 11: From CPU-driven BitBlt source data |

Command Register 1

Register Type: Read/Write

Read/Write Port: 82ABh

Default: 00h

| | |
|--------|---|
| D7 | Hardware Command Queue status 0: Hardware Command queue is not empty 1: Hardware Command queue is empty |
| D6 | Graphics engine status 0: Graphics engine is idle and Hardware command queue is empty 1: Graphics engine is busy or Hardware command queue is not empty |
| D5 | Enhanced Color/Font Expansion 0: Disable enhanced color expansion 1: Enable enhanced color expansion |
| D4 | Software Command Queue Status 0: Software Command queue empty 1: Software Command queue not empty |
| D3 | Line drawing last pixel control 0: Last pixel will be drawn 1: Last pixel will not be drawn |
| D2 | Line drawing major axial selection 0: Y-axial is major 1: X-axial is major |
| D[1:0] | Command type select bit 1-0 00: Bitblt 01: BitBlt with mask 10: Color/Font expansion 11: Line drawing |

NOTE: Word_writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.



6.8.3 The Register Format for Direct Draw

The register format for Direct Draw is shown in following table.

| | | | | |
|--------------------|-------------------------------------|----------------------|----------|------------|
| D[31:24] | D[23:16] | D[15:08] | D[07:00] | IO Address |
| Reserved | Source Start Linear Address | | | 8280h |
| Reserved | Destination Start Linear Address | | | 8284h |
| Destination Pitch | | Source Pitch | | 8288h |
| Rectangular Height | | Rectangular Width | | 828Ch |
| S Alpha Bit | High Value of Source Color Key | | | 8290h |
| D Alpha Bit | High value of Destination Color Key | | | 8294h |
| D Rop | Low Value of Source Color Key | | | 8298h |
| Reserved | Low Value of Destination Color Key | | | 829Ch |
| Top Clipping | | Left Clipping | | 82A0h |
| Bottom Clipping | | Right Clipping | | 82A4h |
| Command/Status | | Command Queue Status | | 82A8h |

Source Start Linear Address

Register Type: Read/Write
 Read/Write Port: 8280h~8283h
 Default: 00h

D[31:22] Reserved
 D[21:0] Source Start Linear Address Bit[21:0]

Destination Start Linear Address

Register Type: Read/Write
 Read/Write Port: 8284h~8287h
 Default: 00h

D[31:22] Reserved
 D[21:0] Destination Start Linear Address Bit[21:0]

Source Pitch

Register Type: Read/Write
 Read/Write Port: 8288h~8289h
 Default: 00h

D[15:12] Reserved
 D[11:0] Source Pitch Bit[11:0]

Destination Pitch

Register Type: Read/Write
 Read/Write Port: 828Ah~828Bh
 Default: 00h

D[15:12] Reserved
 D[11:0] Destination Pitch Bit[11:0]

Rectangular Width

Register Type: Read/Write
 Read/Write Port: 828Ch~828Dh
 Default: 00h



D[15:12] Reserved
D[11:0] Destination Rectangular Width Bit[11:0]

Rectangular Height

Register Type: Read/Write
Read/Write Port: 828Eh~828Fh
Default: 00h
D[15:12] Reserved
D[11:0] Destination Rectangular Height Bit[11:0]

High value of Source Color Key

Register Type: Read/Write
Read/Write Port: 8290h~8292h
Default: 00h
D[23:0] High Value of Source Color Key Bit[23:0]

Alpha Blending Control Bit for Source Color (S_Alpha Bit)

Register Type: Read/Write
Read/Write Port: 8293h
Default: 00h
D[7:1] Reserved
D0 Control Bit for Source Color Alpha Blending

High Value of Destination Color Key (D_Alpha Bit)

Register Type: Read/Write
Read/Write Port: 8294h~8296h
Default: 00h
D[23:0] High Value of Destination Color Key Bit[23:0]

Alpha Blending Control Bit for Destination Color (D_Alpha Bit)

Register Type: Read/Write
Read/Write Port: 8297h
Default: 00h
D[7:1] Reserved
D0 Control Bit for Destination Color Alpha Blending

Low Value of Source Color Key

Register Type: Read/Write
Read/Write Port: 8298h~829Ah
Default: 00h
D[23:0] Low Value of Source Color Key Bit[23:0]

Direct Draw Rop (D_Rop)

Register Type: Read/Write
Read/Write Port: 829Bh
Default: 00h
D[7:4] Reserved
D[3:0] Direct Draw Raster Operation Bit[3:0]

**Low Value of Destination Color Key**

Register Type: Read/Write
Read/Write Port: 829Ch~829Fh
Default: 00h
D[23:0] Low Value of Destination Color Key Bit[23:0]

Left Clipping

Register Type: Read/Write
Read/Write Port: 82A0h~82A1h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Left Bit[11:0]

Top Clipping

Register Type: Read/Write
Read/Write Port: 82A2h~82A3h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Top Bit[11:0]

Right Clipping

Register Type: Read/Write
Read/Write Port: 82A4h~82A5h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Right Bit[11:0]

Bottom Clipping

Register Type: Read/Write
Read/Write Port: 82A6h~82A7h
Default: 00h
D[15:12] Reserved
D[11:0] Rectangular Clipping Bottom Bit[11:0]

Command Queue Status

Register Type: Read/Write
Read/Write Port: 82A8h~82A9h
Default: 00h

If Hardware Command Queue is enable, then

D[15:5] reserved
D[4:0] Available Command Queue Length Bit[4:0]

If Turbo Queue is enable, then

D[15:0] Head/Tail Index Bit[15:0]

The Head Index is written into this register, and the Tail Index is read from this registers.

**Command Register 0**

Register Type: Read/Write

Read/Write Port: 82AAh

Default: 00h

| | |
|--------|---|
| D7 | Rectangular Clipping Mode 0: Clipping internal region 1: Clipping external region |
| D6 | Rectangular Clipping Control 0: Disable rectangular clipping logic 1: Enable rectangular clipping logic |
| D5 | Y direction control 0: Y counter decrease 1: Y counter increase |
| D4 | X direction control 0: X counter decrease 1: X counter increase |
| D[3:2] | Direct Draw Enable 00: Reserved 01: Reserved 10: Reserved 11: Enable Direct Draw The two bits (D[3:2]) must be set to “11” then the Direct Draw function can be enabled. |
| D[1:0] | Source select bit 1-0 00: From background color registers 01: From foreground color registers 10: From video memory 11: From CPU-driven BitBlt Source Data |

Command Register 1

Register Type: Read/Write

Read/Write Port: 82ABh

Default: 00h

| | |
|----|---|
| D7 | Hardware Command Queue status 0: Hardware Command queue is not empty 1: Hardware Command queue is empty |
| D6 | Graphics engine status 0: Graphics engine is idle and Hardware command queue is empty 1: Graphics engine is busy or Hardware command queue is not empty |
| D5 | Enhanced Color/Font Expansion 0: Disable enhanced color expansion 1: Enable enhanced color expansion |
| D4 | Software Command Queue Status 0: Software Command queue empty 1: Software Command queue not empty |
| D3 | Line drawing last pixel control 0: Last pixel will be drawn |



D2 1: Last pixel will not be drawn
Line drawing major axial selection
0: Y-axial is major
1: X-axial is major

D[1:0] Command type select bit 1-0
00: Bitblt
01: BitBlt with mask
10: Color/Font expansion
11: Line drawing

NOTE: Word_writing to Command 1 and Command 0, it will automatically initiate graphics engine to execute the specified command.



6.9 Video Accelerator Registers

| Index(3D4) | Video Accelerator Register (3D5) |
|------------|--|
| 80h | Password/Identification Register |
| 81h | Video Window Horizontal Display Start Low Register |
| 82h | Video Window Horizontal Display End Low Register |
| 83h | Video Window Horizontal Display Overflow Register |
| 84h | Video Window Vertical Display Start Low Register |
| 85h | Video Window Vertical Display End Low Register |
| 86h | Video Window Vertical Display Overflow Register |
| 87h | Video Capture Frame Buffer Starting Address Low Register |
| 88h | Video Capture Frame Buffer Starting Address Middle Register |
| 89h | Video Frame Buffer Overflow Register |
| 8Ah | Video Display Frame Buffer Starting Address Low Register |
| 8Bh | Video Display Frame Buffer Starting Address Middle Register |
| 8Ch | Video Frame Buffer Offset Low Register |
| 8Dh | Video Display Frame Buffer End Address Low Register |
| 8Eh | Video Frame Buffer Offset Address High Register |
| 8Fh | Video Capture Threshold Value Register |
| 90h | Video Capture Horizontal Down Scaling Factor Register |
| 91h | Video Capture Vertical Down Scaling Register |
| 92h | Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register |
| 93h | Vertical Up Scaling Factor Register |
| 94h | Horizontal Scaling Factor Integer Register |
| 95h | Video Overlay Color Key Blue Low Value Register |
| 96h | Video Overlay Color Key Green Low Value Register |
| 97h | Video Overlay Color Key Red Low Value Register |
| 98h | Video Control Misc. Register 0 |
| 99h | Video Control Misc. Register 1 |
| 9Ah | Video Chroma Key B/Y Low Value Register |
| 9Bh | Video Chroma Key G/U Low Value Register |
| 9Ch | Video Chroma Key R/V Low Value Register |
| 9Dh | Video Control Misc. Register 3 |
| 9Eh | Video Playback Threshold Low Value Register |
| 9Fh | Video Playback Threshold High Value Register |
| A0h | Line Buffer Size Register |
| A1h | Video Overlay Color Key Blue High Value Register |
| A2h | Video Overlay Color Key Green High Value Register |
| A3h | Video Overlay Color Key Red High Value Register |
| A4h | Video Chroma Key B/Y High Value Register |
| A5h | Video Chroma Key G/U High Value Register |
| A6h | Video Chroma Key R/V High Value Register |
| A7h | Graphics Data Alpha Value Register |
| A8h | Video Data Alpha Value Register |
| A9h | Key Overlay Operation Mode Register |



| | |
|-----|--|
| AAh | Video Capture Horizontal Start Register |
| ABh | Video Capture Horizontal End Register |
| ACh | Video Capture Vertical Start Register |
| ADh | Video Capture Vertical End Register |
| AEh | Video Capture Horizontal Overflow Register |
| AFh | Video Capture Vertical Overflow Register |
| B0h | System Memory Video Frame Buffer Setting Register 1 |
| B1h | System Memory Video Frame Buffer Setting Register 2 |
| B2h | System Memory Video Frame Buffer Setting Register 3 and Video Control Register |

6.9.1 Password/Identification Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 80h
Default: 00h

D[7:0] Password/identification Bit[7:0]

Description:

If 86h is written to this register, A1h will be read from this register and all the video extension registers would be unlocked to allow desired change.

If any value other than 86h is written to this register, 21h will be read from this register and all the video extension registers would be locked to prevent unauthorized change.

6.9.2 Video Window Horizontal Display Start Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 81h
Default: 00h

D[7:0] Video window horizontal display start Bit[7:0]

Description:

The Video Window Horizontal Display Start Bit[10:0] form the left boundary of the video window. The Bit[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h, Sec. 6.9.4 on page 100). The boundary is in unit of pixel.

6.9.3 Video Window Horizontal Display End Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 82h
Default: 00h

D[7:0] Video window horizontal display end Bit[7:0]

Description:

The Video Window Horizontal Display End Bit[10:0] form the right boundary of the video window. The Bits[10:8] is located in the Video Window Horizontal Display Overflow Register (Index 83h, Sec. 6.9.4 on page 100). The boundary is in unit of pixel.

6.9.4 Video Window Horizontal Display Overflow Register

Register Type: Read/Write



Read/Write Port: 3D5, Index 83h
Default: 00h

| | |
|--------|---|
| D[2:0] | Video window horizontal display start Bit[10:8] |
| D3 | Reserved |
| D[6:4] | Video window horizontal display end Bit[10:8] |
| D7 | Reserved |

6.9.5 Video Window Vertical Display Start Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 84h
Default: 00h

| | |
|--------|--|
| D[7:0] | Video window vertical display start Bit[7:0] |
|--------|--|

Description:

The Video Window Vertical Display Start Bit[10:0] form the top boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h, 6.9.7 on page 101). The boundary is in unit of line.

6.9.6 Video Window Vertical Display End Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 85h
Default: 00h

| | |
|--------|--|
| D[7:0] | Video window vertical display end Bit[7:0] |
|--------|--|

Description:

The Video Window Vertical Display End Bit[10:0] form the bottom boundary of the video window. The Bit[10:8] is located in the Video Window Vertical Display Overflow Register (Index 86h, 6.9.7 on page 101). The boundary is in unit of line.

6.9.7 Video Window Vertical Display Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 86h
Default: 00h

| | |
|--------|---|
| D[2:0] | Video window horizontal display start Bit[10:8] |
| D3 | Reserved |
| D[6:4] | Video window horizontal display end Bit[10:8] |
| D7 | Reserved |

6.9.8 Video Capture Frame Buffer Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 87h
Default: 00h

| | |
|--------|--|
| D[7:0] | Video capture frame buffer starting address Bit[7:0] |
|--------|--|

Description:

The Video Capture Frame Buffer Starting Address Bit[19:0] form the video frame buffer starting address in unit of doubleword. The Bit[15:8] are located in the Video Capture Frame Buffer Starting Address Middle Register (Index 88h, Sec. 6.9.9 on page 102). The



Bit[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h, Sec. 6.9.10 on page 102).

6.9.9 Video Capture Frame Buffer Starting Address Middle Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 88h
Default: 00h

D[7:0] Video capture frame buffer starting address Bit[15:8]

6.9.10 Video Frame Buffer Overflow Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 89h
Default: 00h

D[3:0] Video capture frame buffer starting address Bit[19:16]

D[7:4] Video display frame buffer starting address Bit[19:16]

6.9.11 Video Display Frame Buffer Starting Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Ah
Default: 00h

D[7:0] Video display frame buffer starting address Bit[7:0]

Description:

The Video Display Frame Buffer Starting Address Bit[19:0] form the video display starting address in unit of doubleword. The Bit[15:8] are located in the Video Display Frame Buffer Starting Address Middle Register (Index 8Bh, Sec.6.9.12 on page 102). The Bits[19:16] are located in the Video Frame Buffer Overflow Register (Index 89h, Sec. 6.9.10 on page 102).

This address could be different from the video capture frame buffer starting address to perform the video display panning function.

6.9.12 Video Display Frame Buffer Starting Address Middle Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Bh
Default: 00h

D[7:0] Video display frame buffer starting address Bit[15:8]

6.9.13 Video Frame Buffer Offset Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Ch
Default: 00h

D[7:0] Video frame buffer offset Bit[7:0]

Description:

The Video Frame Buffer Offset Bit[11:0] form the offset of the video frame buffer. The Bit[11:8] are located in the Video Frame Buffer Offset High Register (Index 8Eh, Sec. 6.9.15 on page 103).



The offset defines the size of the scan line of the video data captured in the video frame buffer in unit of double word. It should slightly larger than the actual size of captured video image to avoid the data over stored to next scan line buffer.

6.9.14 Video Display Frame Buffer End Address Low Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Dh
Default: 00h

D[7:0] Video display frame buffer end address Bit[7:0]

Description:

The Video Capture Frame Buffer End Address Bit[7:0] form the end address of the video frame buffer. The address is in unit of 16k bytes. This address defines the end address of the capture frame buffer. It can prevent the captured data to destroy the other data outside the capture frame buffer when the video data input is unstable.

6.9.15 Video Frame Buffer Offset Address High Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Eh
Default: 00h

D[3:0] Video frame buffer offset Bit[11:8]
D[7:4] Reserved

6.9.16 Video Capture Threshold Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 8Fh
Default: 00h

D[2:0] Video capture threshold low Bit[2:0]
D3 Reserved
D[6:4] Video capture threshold high Bit[2:0]
D7 Reserved

Description:

This register contains the video capture FIFO threshold low and the video capture FIFO threshold high.

The threshold low defines the FIFO lower boundary which indicates the FIFO is full enough and the data in the FIFO can be written into the DRAM. But if the priority of the threshold low is lower than others, it can wait until it is able to write the data of FIFO into the DRAM.

The threshold high defines the FIFO upper boundary which indicates the FIFO is about to be overflow and the data of the FIFO must be written into the DRAM as soon as possible.

These two thresholds should be modified to catch the maximum performance by compromising with the CRT threshold, video display threshold, and DRAM refresh rate, etc.

6.9.17 Video Capture Horizontal Down Scaling Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 90h



Default: 00h
D[5:0] Video capture horizontal down scaling factor Bit[5:0]
D[7:6] Reserved

Description:

This register contains the video capture horizontal down scaling factor (HDSF). The horizontal size of the captured video frame will be scaled to $(64-HDSF)/64$. Since the scaled-down video frame maybe will not fit into the video display window, the margins outside the video display window will be cut off. This factor is not only used to fit the window size but also is used to reduce the bandwidth required for the video capture and video display.

6.9.18 Video Capture Vertical Down Scaling Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 91h
Default: 00h
D[5:0] Vertical down scaling factor Bit[5:0]
D[7:6] Reserved

Description:

This register contains the video capture vertical down scaling factor (VDSF). The vertical size of the captured video frame will be scaled to $(64-VDSF)/64$. Since the scaled-down video frame maybe will not fit into the video display window, the margins outside the video display window will be cut off. This factor is not only used to fit the window size but also is used to reduce the bandwidth required for the video capture and video display.

6.9.19 Horizontal Up Scaling Factor and Horizontal Interpolation Accuracy Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 92h
Default: 00h
D[5:0] Horizontal up scaling factor Bit[5:0]
D[7:6] Horizontal up-scaling interpolation accuracy factor
00: replication
01: 2-phase
10: 4-phase
11: 8-phase

Description:

This field contains the video playback horizontal up scaling factor fraction (HSFF). It is combined with the horizontal scaling factor integer (HSFI) register (Index 94h, Sec 6.9.21 on page 105) to form horizontal scaling. The horizontal size will be scaled to $1/(HSFI+(HSFF/64))$. The HSFI should be zero for up-scaling. The HSFI should not be zero for down-scaling.

The Up-scaling interpolation accuracy factor can modify the up-scaling interpolation DDA accuracy phases.

6.9.20 Vertical Up Scaling Factor Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 93h
Default: 00h



| | |
|--------|---|
| D[5:0] | Vertical up scaling factor Bit[5:0] |
| D[7:6] | Video frame buffer data format selection Bit[1:0] |
| | for YUV format, |
| | 00: UYVY 4:2:2 |
| | 01: VYUY 4:2:2 |
| | 10: YUYV 4:2:2 |
| | 11: YVYU 4:2:2 |
| | for RGB format, |
| | 00: RGB 5:5:5 |
| | 01: RGB 5:6:5 |

Description:

This field contains the video playback vertical up scaling factor (VUSF). The vertical size will be scaled to 64/VUSF. If VUSF=0, the vertical size will not be scaled.

6.9.21 Horizontal Scaling Factor Integer Register

Register Type : Read/Write
Read/Write Port : 3D5, Index 94h

| | |
|--------|--|
| D[3:0] | Horizontal Scaling Factor Integer Bit[3:0] |
| D[7:4] | Reserved |

6.9.22 Video Overlay Color Key Blue Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 95h
Default: 00h

| | |
|--------|-------------------|
| D[7:0] | Blue Key Bit[7:0] |
|--------|-------------------|

Description:

This register contains the blue video overlay color key low value.

In 8-bit color mode, it is used as the color key low value.

In 16-bit color mode, it is used as the low byte of color key low value.

In 24-bit color mode, it is used as the blue byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

6.9.23 Video Overlay Color Green Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 96h
Default: 00h

| | |
|--------|--------------------|
| D[7:0] | Green Key Bit[7:0] |
|--------|--------------------|

Description:

This register contains the green video overlay color key low value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is used as the high byte of color key low value.

In 24-bit color mode, it is used as the green byte of the color key low value.



If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

6.9.24 Video Overlay Color Red Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 97h
Default: 00h

D[7:0] Red Key Bit[7:0]

Description:

This register contains the red video overlay color key low value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is invalid.

In 24-bit color mode, it is used as the red byte of the color key low value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

6.9.25 Video Control Misc. Register 0

Register Type: Read/Write
Read/Write Port: 3D5, Index 98h
Default: 00h

D0 Enable video capture
0: Disable video capture
1: Enable video capture

This bit could enable the video capture. If the video data is input through feature connector (FC), this bit should be set. The video pause function can be performed by disable this bit but enable the video playback bit.

D1 Enable video playback
0: Disable video playback
1: Enable video playback

This bit could enable the video playback. When the data of the video frame buffer are fetched by the system, the bandwidth of DRAM maybe not enough. The video playback can be disabled to gain the bandwidth but the video will not be played back.

D2 Reserved

D3 Reserved

D4 Video only display mode
0: Disable video only display mode
1: Enable video only display mode

The graphics display can be disable by setting this bit. This can reduce the DRAM bandwidth especially on the full screen video playback mode.

D5 Video capture interlace control
0: Disable video capture interlace control
1: Enable video capture interlace control



- The video data input through feature connector could be interlaced. If the input video data are interlaced this bit should be set.
- D6 Video format selection
0: Select RGB format
1: Select YUV format
This bit is used with the video frame buffer data format selection field of register CR92 to select the correct video data format.
- D7 Field Polarity Selection
0: Select Odd/*Even
1: Select *Odd/Even
This bit can select the polarity of Field signal.

6.9.26 Video Control Misc. Register 1

- Register Type: Read/Write
Read/Write Port: 3D5, Index 99h
Default: 00h
- D0 Enable YUV data capture
0: Capture RGB format video data
1: Capture YUV format video data
The video capture can be RGB and YUV format.
- D1 Enable dithering
0: Disable dithering
1: Enable dithering
The captured video data can be dithered for better video quality.
- D2 Capture format select
0: Format RGB 565
1: Format RGB 555
The capture video data may be RGB 555 or RGB565 format.
- D[5:3] Horizontal filter select
000: 1
001: $(1/8(1+3z^{-1}+3z^{-2}+z^{-3}))$
010: $(1/4(1+2z^{-1}+z^{-2}))$
011: $(1/2(1+z^{-1}))$
others: Reserved
- D6 Enable vertical sync. interrupt
0: Disable
1: Enable
The video input vertical sync. signal could cause interrupt when this bit is enabled.
- D7 Clear vertical sync. interrupt
0: Disable
1: Enable
After the vertical sync. caused an interrupt, this bit should be set for clear the interrupt request.

6.9.27 Video Chroma Key B/Y Low Value Register

- Register Type: Read/Write
Read/Write Port: 3D5, Index 9Ah



Default: 00h
D[7:0] Video Chroma B/Y Key Low Bit[7:0]

Description:

This register contains the blue or Y video overlay chroma key low value.
In RGB chroma key mode, it is used as the blue byte of the chroma key low value.
In YUV chroma key mode, it is used as the Y of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

6.9.28 Video Chroma Key G/U Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Bh
Default: 00h
D[7:0] Video Chroma G/U Key Low Bit[7:0]

Description:

This register contains the green or U video overlay chroma key low value.
In RGB chroma key mode, it is used as the green byte of the chroma key low value.
In YUV chroma key mode, it is used as the U of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

6.9.29 Video Chroma Key R/V Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Ch
Default: 00h
D[7:0] Video Chroma R/V Key Low Value Bit[7:0]

Description:

This register contains the red or V video overlay chroma key low value.
In RGB chroma key mode, it is used as the red byte of the chroma key low value.
In YUV chroma key mode, it is used as the V of the chroma key low value.
If the value of the video data is greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

6.9.30 Video Control Misc. Register 3

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Dh
Default: 00h
D7 Enable system memory video frame buffer
0: Disable
1: Enable

The captured frame buffer can be placed on system memory.
But this mode can only be enabled under shared-memory architecture.



| | |
|----|---|
| D6 | Support for Brooktree Bt819A video decoder SPI mode 1 0: Disable 1: Enable |
| D5 | Enable VMI interrupt 0: Disable 1: Enable The VMI device could cause interrupt when this bit is enabled. |
| D4 | Enable VMI interface 0: Disable 1: Enable |
| D3 | Enable VMI device access 0: Disable 1: Enable |
| D2 | Chroma Key Format selection 0: RGB format 1: YUV format |
| D1 | UV format select for video playback 0: CCIR 601 format 1: 2's complement format |
| D0 | UV format select for video capture 0: CCIR 601 format 1: 2's complement format |

6.9.31 Video Playback Threshold Low Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Eh
Default: 00h

D7 Reserved
D[6:0] Video capture threshold low Bit[6:0]

Description:

This register contains the video line buffer threshold low.
The threshold low defines the video line buffer lower boundary which indicates the line buffer is not enough and the video data should be read from the DRAM.

6.9.32 Video Playback Threshold High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index 9Fh
Default: 00h

D7 Reserved
D[6:0] Video capture threshold high Bit[6:0]

Description:

This register contains the video line buffer threshold high.
The threshold high defines the video line buffer upper boundary which indicates the data in the video line buffer is enough.



These two thresholds (video playback threshold low and threshold high) should be modified to get the maximum performance by compromising with the CRT threshold, video capture threshold, and DRAM refresh rate, etc.

6.9.33 Line Buffer Size Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A0h
Default: 00h

D[7:0] Line Buffer Size Bit[7:0]

Description:

This register should be set to the line buffer size used by playback. The size is in unit of quad-word.

6.9.34 Video Overlay Color Key Blue High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A1h
Default: 00h

D[7:0] Blue Key High Value Bit[7:0]

Description:

This register contains the blue video overlay color key high value.

In 8-bit color mode, it is used as the color key high value.

In 16-bit color mode, it is used as the low byte of color key high value.

In 24-bit color mode, it is used as the blue byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

6.9.35 Video Overlay Color Key Green High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A2h
Default: 00h

D[7:0] Green Key High Value Bit[7:0]

Description:

This register contains the green video overlay color key high value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is used as the high byte of color key high value.

In 24-bit color mode, it is used as the green byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

6.9.36 Video Overlay Color Key Red High Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A3h
Default: 00h



D[7:0] Red Key High Value Bit[7:0]

Description:

This register contains the red video overlay color key high value.

In 8-bit color mode, it is invalid.

In 16-bit color mode, it is invalid.

In 24-bit color mode, it is used as the red byte of the color key high value.

If the value of the graphics data is greater than or equal to the color key low value, and lower than or equal to the color key high value, the graphics data may be replaced by video data in the way defined by key operation mode.

6.9.37 Video Chroma Key B/Y High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A4h

Default: 00h

D[7:0] Video Chroma B/Y Key High Value Bit[7:0]

Description:

This register contains the blue or Y video overlay chroma key high value.

In RGB chroma key mode, it is used as the blue byte of the chroma key high value.

In YUV chroma key mode, it is used as the Y of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

6.9.38 Video Chroma Key G/U High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A5h

Default: 00h

D[7:0] Video Chroma G/U Key High Value Bit[7:0]

Description:

This register contains the green or U video overlay chroma key high value.

In RGB chroma key mode, it is used as the green byte of the chroma key high value.

In YUV chroma key mode, it is used as the U of the chroma key high value.

If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced by graphics data in the way defined by key operation mode.

6.9.39 Video Chroma Key R/V High Value Register

Register Type: Read/Write

Read/Write Port: 3D5, Index A6h

Default: 00h

D[7:0] Video Chroma R/V Key High Value Bit[7:0]

Description:

This register contains the red or V video overlay chroma key high value.

In RGB chroma key mode, it is used as the red byte of the chroma key high value.

In YUV chroma key mode, it is used as the V of the chroma key high value.



If the value of the video data is the greater than or equal to the chroma key low value, and lower than or equal to the chroma key high value, the video data may be replaced graphics data in the way defined by key operation mode.

6.9.40 Graphics Data Alpha Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A7h
Default: 00h

D[7:0] Graphics Data Alpha Value Bit[7:0]

Description:

The pixels of graphics data can be blended by graphics data alpha value, then added with the blended video data to generates blended data. The accuracy of the blending is 3 bits, the 3 MSBs of this register.

6.9.41 Video Data Alpha Value Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A8h
Default: 00h

D[7:0] Video Data Alpha Value Bit[7:0]

Description:

The pixels of video data can be blended by video data alpha value, then added with the blended graphics data to generates blended data. The accuracy of the blending is 3 bits, the 3 MSBs of this register.

6.9.42 Key Overlay Operation Mode Register

Register Type: Read/Write
Read/Write Port: 3D5, Index A9h
Default: 00h

D[7:4] Reserved

D[3:0] Key Overlay Operation Mode Bit[3:0]

Description:

There are two keys for graphics data and video data overlay, which are color key and chroma key. The key overlay operation mode indicates the way the overlay would be performed.

| Operation Mode | Operation |
|----------------|---|
| 0000 | always select graphics data |
| 0001 | select blended data when color key and chroma key, otherwise select graphics data |
| 0010 | select blended data when color key and not chroma key, otherwise select graphics data |
| 0011 | select blended data when color key, otherwise select graphics data |
| 0100 | select blended data when not color key and chroma key, otherwise select graphics data |



| | |
|------|--|
| 0101 | select blended data when chroma key, otherwise select graphics data |
| 0110 | select blended data when color key xor chroma key, otherwise select graphics data |
| 0111 | select blended data when color key or chroma key, otherwise select graphics data |
| 1000 | select blended data when not color key and not chroma key, otherwise select graphics data |
| 1001 | select blended data when color key xnor chroma key, otherwise select graphics data |
| 1010 | select blended data when not chroma key, otherwise select graphics data |
| 1011 | select blended data when color key or not chroma key, otherwise select graphics data |
| 1100 | select blended data when not chroma key, otherwise select graphics data |
| 1101 | select blended data when not color key or chroma key, otherwise select graphics data |
| 1110 | select blended data when not color key or not chroma key, otherwise select graphics data |
| 1111 | always select blended data |

6.9.43 Video Capture Horizontal Start Register

Register Type: Read/Write
Read/Write Port: 3D5, Index AAh
Default: 00h

D[7:0] Video Capture Horizontal Start Bit[7:0]

Description:

The Video Capture Horizontal Start Bit[10:0] indicate the left boundary of the captured video data. The Bit[10:8] is located in the Video Capture Horizontal Overflow Register (Sec. 6.9.47 on page 115, Index AEh). The boundary is counted by the input video data clock. When the signal BLANK* is valid, the video data horizontal counter starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

Note: This register should be set to zero at Brooktree BT819A video decoder SPI mode 2.

6.9.44 Video Capture Horizontal End Register

Register Type: Read/Write
Read/Write Port: 3D5, Index ABh
Default: 00h



D[7:0] Video Capture Horizontal End Bit[7:0]

Description:

The Video Capture Horizontal End Bit[10:0] indicate the right boundary of the captured video data. The Bit[10:8] is located in the Video Capture Horizontal Overflow Register (Sec. 6.9.47 on page 115, Index AEh). The boundary is counted by the input video data clock. When the signal BLANK* is valid, the video data horizontal counter starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

6.9.45 Video Capture Vertical Start Register

Register Type: Read/Write
Read/Write Port: 3D5, Index ACh
Default: 00h

D[7:0] Video Capture Vertical Start Bit[7:0]

Description:

The Video Capture Vertical Start Bit[9:0] indicate the upper boundary of the captured video data. The Bit[9:8] is located in the Video Capture Vertical Overflow Register (Sec. 6.9.48 on page 115, Index AFh). The boundary is counted by the input video data clock. In the positive edge of the signal VDVSYNC, the video data vertical counter would be reset and then starts to count.

The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

6.9.46 Video Capture Vertical End Register

Register Type: Read/Write
Read/Write Port: 3D5, Index ADh
Default: 00h

D[7:0] Video Capture Vertical End Bit[7:0]

Description:

The Video Capture Vertical End Bit[9:0] indicate the upper boundary of the captured video data. The Bit[9:8] is located in the Video Capture Vertical Overflow Register (Sec. 5.9.48, Index AFh). The boundary is counted by the input video data clock. In the positive edge of the signal VDVSYNC, the video data vertical counter would be reset and then starts to count.



The video data capture would be started or continued when the video data horizontal counter is equal to or greater than the Video Capture Horizontal Start and the video data vertical counter is equal to or greater than the Video Capture Vertical Start.

The video data capture would be ended when the video data horizontal counter is equal to or greater than the Video Capture Horizontal End or the video data vertical counter is equal to or greater than the Video Capture Vertical End.

6.9.47 Video Capture Horizontal Overflow Register

| | |
|------------------|--|
| Register Type: | Read/Write |
| Read/Write Port: | 3D5, Index AEh |
| Default: | 00h |
| D7 | Reserved |
| D[6:4] | Video Capture Horizontal End Bit[10:8] |
| D3 | Reserved |
| D[2:0] | Video Capture Horizontal Start Bit[10:8] |

6.9.48 Video Capture Vertical Overflow Register

| | |
|------------------|--|
| Register Type: | Read/Write |
| Read/Write Port: | 3D5, Index AFh |
| Default: | 00h |
| D7 | Video Input Clock Selection 0: The video clock input from pin PCLK 1: The video clock input from pin LLC1 The input video data clock could come from pin PCLK or LLC1 for flexible application circuit design. |
| D[6:4] | Video Data Input Delay Compensation Bit[2:0] 000: no delay 001: 2ns 010: 4ns 011: 6ns 100: inversed 101: 2ns, inversed 110: 4ns, inversed 111: 6ns, inversed This field is programmed for input video data clock and input video data delay compensation. |
| D[3:2] | Video Capture Vertical End Bit[9:8] |
| D[1:0] | Video Capture Vertical Start Bit[9:8] |

6.9.49 System Memory Video Frame Buffer Setting Register 1

| | |
|------------------|--|
| Register Type: | Read/Write |
| Read/Write Port: | 3D5, Index B0h |
| Default: | 00h |
| D[7:4] | System Memory Video Frame Buffer Scrambling Table Register Bit[3:0] This field indicates the type of DRAM which the video frame buffer is located. For detail Scrambling Table, refer to page 27. |



| | |
|--------|---|
| D[3:2] | System Memory Video Frame Buffer Row Selection Register Bit[7:0] 00: Row Address [11:0]=memory address[20:9] 01: Row Address [11:0]=memory address[21:10] 10: Row Address [11:0]=memory address[22:11] 11: Row Address [11:0]=memory address[23:12] |
| D1 | Reserved |
| D0 | Reserved |

6.9.50 System Memory Video Frame Buffer Setting Register 2

Register Type: Read/Write
Read/Write Port: 3D5, Index B1h
Default: 00h

| | |
|--------|---|
| D[7:0] | System Memory Video Frame Buffer Segment Register Bit[7:0] The System Memory Video Frame Buffer Segment Register indicates the location of video frame buffer in one specified bank of DRAM. The unit is 256k in 32-bit DRAM bus. The unit is 512k in 64-bit DRAM bus. |
|--------|---|

6.9.51 System Memory Video Frame Buffer Setting Reg. 3 and Video Control Reg.

Register Type: Read/Write
Read/Write Port: 3D5, Index B2h
Default: 00h

| | |
|--------|--|
| D7 | Reserved |
| D6 | Swap YOE* and UVOE* function 0: Disable 1: Enable |
| D5 | Enable YOE* and UVOE* output. 0: Disable 1: Enable |
| D4 | Support for Brooktree BT819A video decoder SPI mode 2 0: Disable 1: Enable |
| D3 | System Memory Video Frame Buffer CAS Selection Register Bit[3:0] 0: Select CASA[7:0] 1: Select CASB[7:0] |
| D2 | System Memory Video Frame Buffer DRAM Type Selection 0: Fast Page DRAM 1: EDO DRAM |
| D[1:0] | System Memory Video Frame Buffer RAS Selection Register Bit[1:0] 00: Select RAS0 01: Select RAS1 10: Select RAS2 11: Select RAS3 |

Description:

The value of the System Memory Video Frame Buffer Setting Registers depends on the DRAM type, DRAM bank, and video frame buffer location.



6.10 PCI Configuration Registers

6.10.1 Configuration Register 00h

Register Type: Read
Read Port: 0000h
Default: 02051039h

D[31:16] Device ID
SiS 6205 Device ID is 0205h

D[15:0] Vendor ID
Integrated Vendor ID is 1039h

6.10.2 Configuration Register 04h

Register Type: Read/Write
Read Port: 0004h
Default: 02000000h

D[26:25] DEVSEL* timing (= 01, Read Only)
00: fast
01: medium (fixed at this value)
10: slow

D5 VGA Palette Snoop
0: Disable
1: Enable

D1 Memory Space
0: Disable
1: Enable

D0 I/O Space
0: Disable
1: Enable

6.10.3 Configuration Register 08h

Register Type: Read
Read Port: 0008h
Default: 03000000h

D[31:8] Class Code (= 030000h)
D[7:0] Revision ID (= Dxh, for Rev. Dx)

6.10.4 Configuration Register 10h

Register Type: Read
Read Port: 0010h
Default: 00000000h

D[31:0] 32-bit memory base register for 4MB linear frame buffer

6.10.5 Configuration Register 14h

Register Type: Read
Read Port: 0014h
Default: 00000000h



D[31:0] 32-bit memory base register for 64KB memory mapped I/O

6.10.6 Configuration Register 18h

Register Type: Read
Read Port: 0018h
Default: 00000001h

D[31:0] 32-bit I/O base register for 16 I/O space which is reserved for VMI interface

6.10.7 Configuration Register 2Ch

Register Type: Read/Write Once Only
Read Port: 002Ch
Default: 00000000h

D[31:16] Subsystem ID
D[15:0] Subsystem Vendor

6.10.8 Configuration Register 30h

Register Type: Read/Write
Read Port: 0030h
Default: 000C0000h

D[31:11] Expansion ROM Base Address
D0 ROM Enable Bit
0: Disable
1: Enable

6.10.9 Configuration Register 3Ch

Register Type: Read
Read Port: 003Ch
Default: 00000100h

If D3 of SRE is 1, then
D[15:8] Interrupt Pin (= 01h, Read Only)
D[7:0] Interrupt Line (= 00h)

If D3 of SRE is 0, then
D[15:8] Interrupt Pin (= 00h, Read Only)
D[7:0] Interrupt Line (= 00h)



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

| Parameter | Min. | Max. | Unit |
|-------------------------------|------|------|------|
| Ambient operation temperature | 0 | 70 | °C |
| Storage temperature | -40 | 125 | °C |
| Input voltage | -0.3 | 5.5 | V |
| Output voltage | -0.5 | 5.5 | V |

NOTE:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

7.2 DC Characteristics

$$T_A = 0 - 70\text{ }^{\circ}\text{C}, V_{DD} = 5\text{ V} \pm 5\%, \text{GND} = 0\text{ V}$$

| Symbol | Parameter | Min. | Max. | Unit | Condition |
|----------|--------------------------|------|----------------|---------------|---------------------------|
| V_{IL} | Input low voltage | -0.5 | 0.8 | V | |
| V_{IH} | Input high voltage | 2.0 | $V_{DD} + 0.5$ | V | |
| V_{OL} | Output low voltage | - | 0.45 | V | $I_{OL} = 4.0\text{ mA}$ |
| V_{OH} | Output high voltage | 2.4 | - | V | $I_{OH} = -1.0\text{ mA}$ |
| I_{IL} | Input leakage current | - | ± 10 | μA | |
| I_{OZ} | Tristate leakage current | - | ± 20 | μA | $0.45 < V_{OUT} < V_{DD}$ |

7.3 DC Characteristics for DAC (Analog Output Characteristics)

| Description | Min. | Typ. | Max. | Unit |
|-------------|------|-------|------|------|
| Black Level | - | 0 | - | V |
| White Level | - | 660 | - | mV |
| ILE | -1.0 | - | +1.0 | LSB |
| DLE | -0.5 | - | +0.5 | LSB |
| 1 LSB | - | 2.625 | - | mV |
| I_{ref} | - | 8.40 | - | mA |

7.4 AC Characteristics for DAC (Analog Output Characteristics)

| Description | Parameter | Condition | Typ. | Max. | Unit |
|---------------|------------|------------------------|------|------|------|
| Settling Time | T_{sett} | R=37.5 ohm C1=30 pF | - | 12.5 | ns |

7.5 AC Characteristics

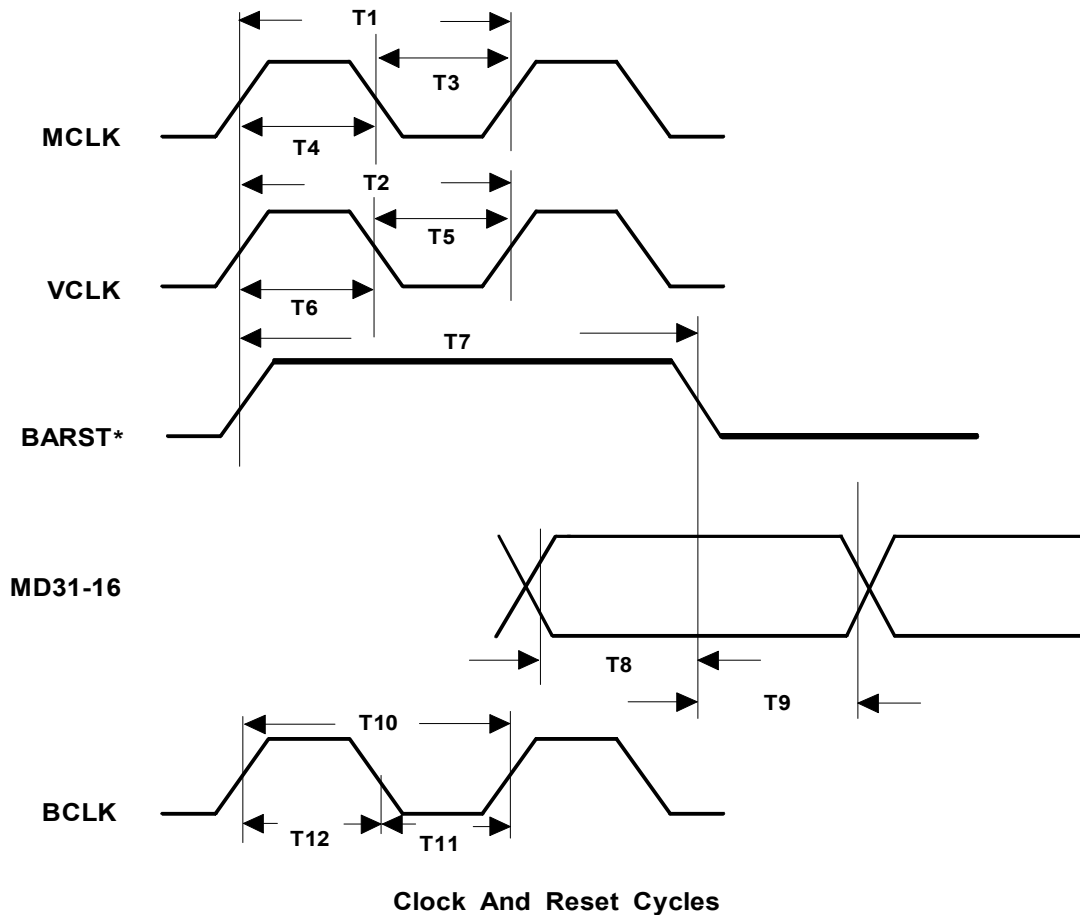
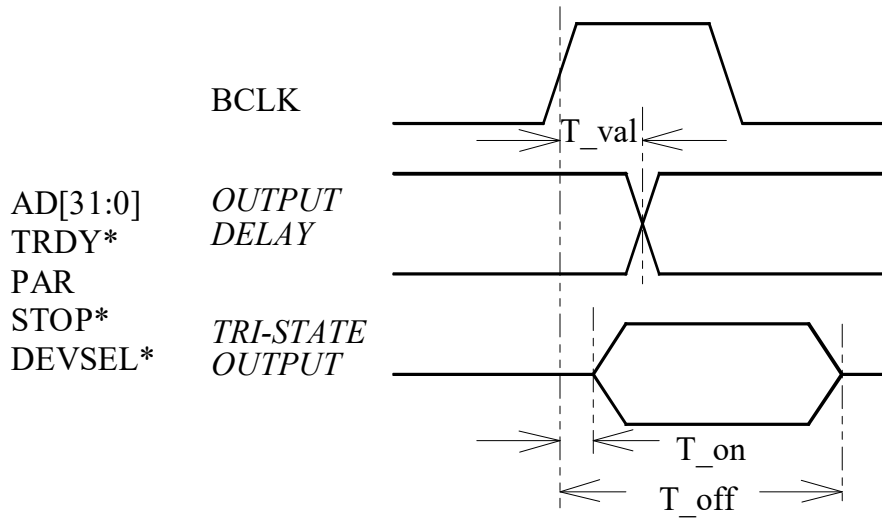
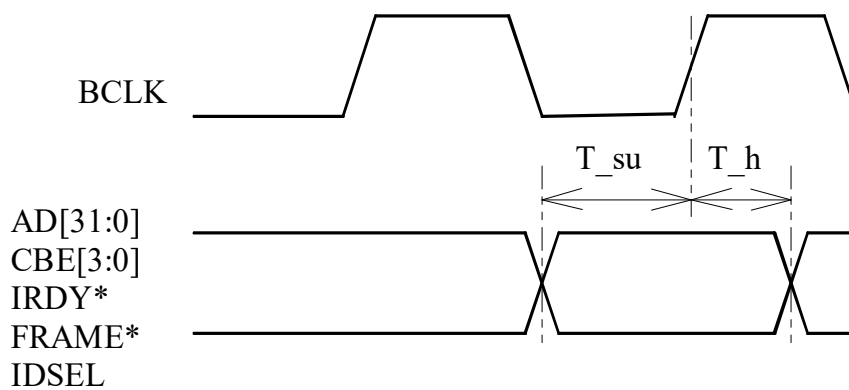


Figure 7.1 Clock and Reset Cycles

Clock and Reset Timing Table

| Symbol | Parameter | Min. | Max. |
|-----------------|--------------------------------------|------|------|
| T ₁ | MCLK Period | 14.3 | |
| T ₂ | VCLK Period | 9 | |
| T ₃ | MCLK Low Time | 6.5 | |
| T ₄ | MCLK High Time | 6.5 | |
| T ₅ | VCLK Low Time | 4 | |
| T ₆ | VCLK High Time | 4 | |
| T ₇ | Reset High Time | 400 | |
| T ₈ | System Configuration Data Setup Time | 20 | |
| T ₉ | System Configuration Data Hold Time | 20 | |
| T ₁₀ | BCLK Period | 30 | |
| T ₁₁ | BCLK High Time | 10 | |
| T ₁₂ | BCLK Low Time | 10 | |

(Units: ns)


Figure 7.2 PCI Output and Tri-state Timing

Figure 7.3 PCI Input Timing
PCI Timing Table

| Symbol | Parameter | Min. | Max. | Units |
|-----------|----------------------------|------|------|-------|
| T_{val} | BCLK to Signal Valid Delay | 2 | 11 | ns |
| T_{on} | Float to Active Delay | 2 | - | ns |
| T_{off} | Active to Float Delay | - | 28 | ns |
| T_{su} | Input Setup Time to BCLK | 7 | - | ns |
| T_h | Input Hold Time from BCLK | 0 | - | ns |

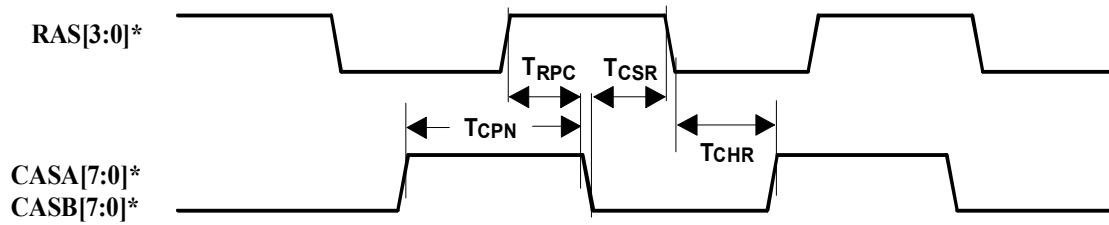


Figure 7.4 CAS Before RAS Refresh Cycle

CAS Before RAS Refresh Cycle Timing Table

| Sym. | Parameter | T-Value | | MCLK 50 MHz | | MCLK 60 MHz | |
|------------------|--------------------------------------|---------|------|----------------|------|----------------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. |
| T _{CPN} | CAS* Precharge Time | 1 | - | 20 | - | 16.7 | - |
| T _{RPC} | RAS* High to CAS* Low Precharge Time | 2 | - | 40 | - | 33.4 | - |
| T _{CSR} | CAS* Before RAS* Setup Time | 1 | - | 20 | - | 16.7 | - |
| T _{CHR} | CAS* Before RAS* Hold Time | 3 | - | 60 | - | 50.1 | - |

(Units: ns)

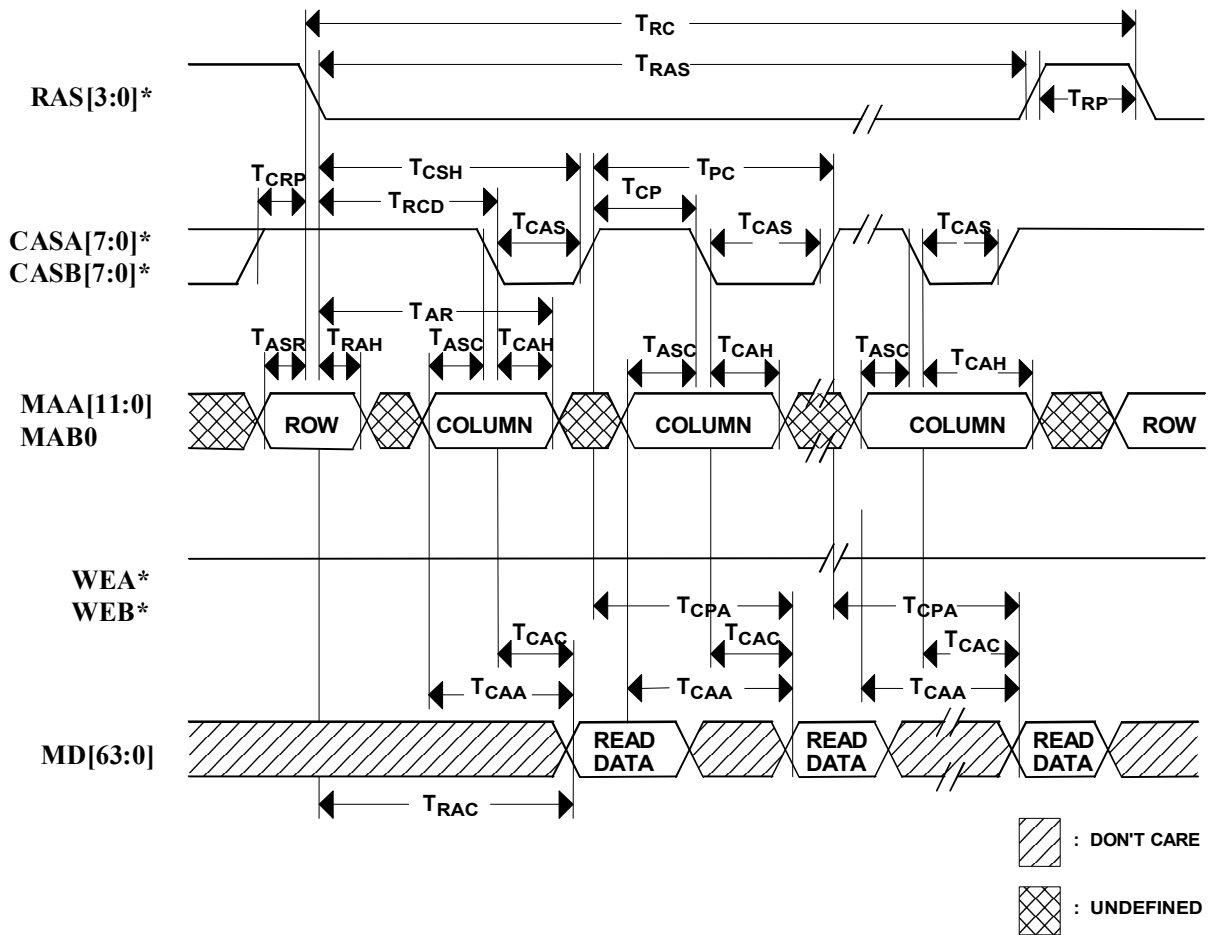


Figure 7.5 Video Memory Fast Page Mode Read Cycle

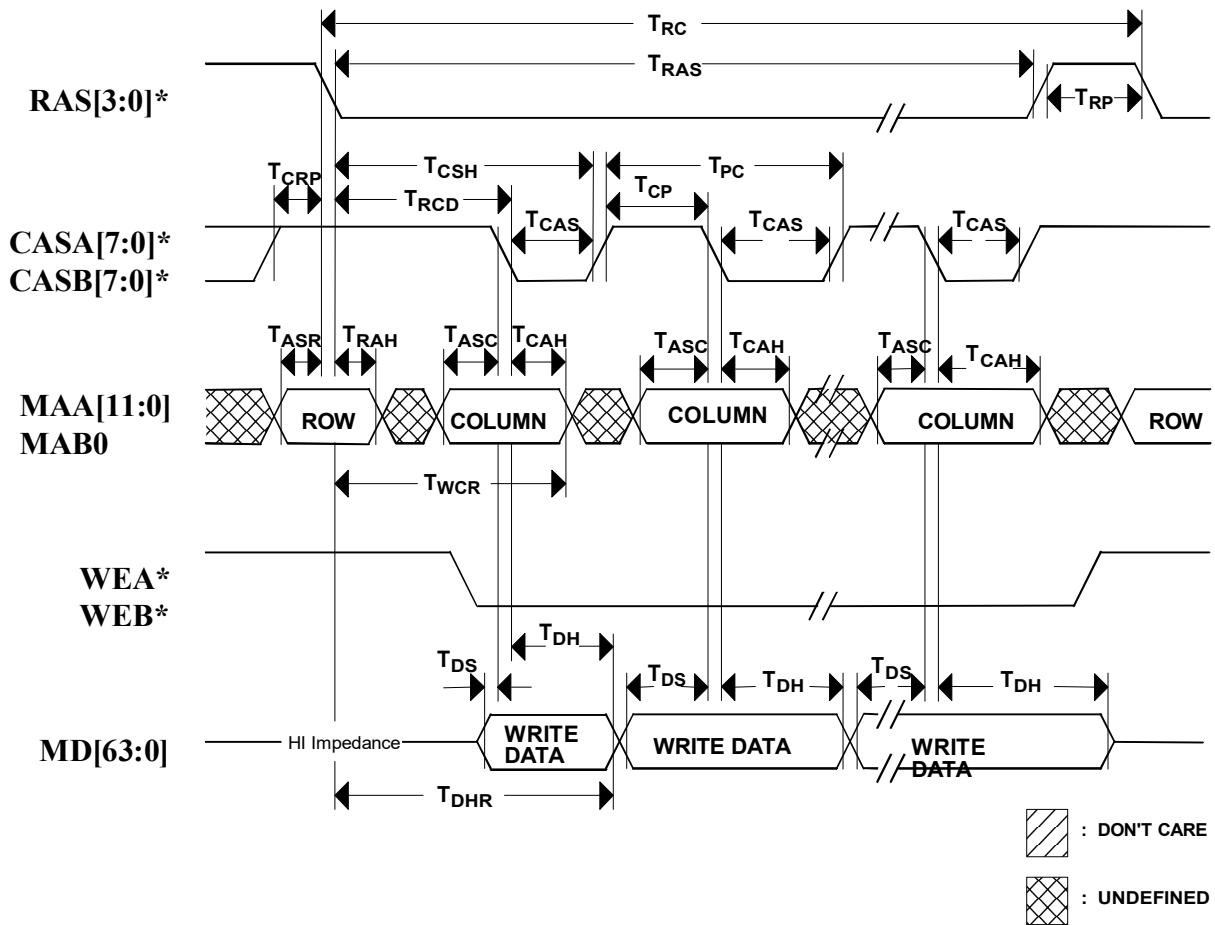


Figure 7.6 Video Memory Fast Page Mode Write Cycle



Video Memory Fast Page Mode Read/Write Cycle Timing Table

Guaranteed Timings

| Sym. | Parameter | T-Value | | MCLK 50 MHz | | MCLK 60 MHz | |
|------|---|---------|------|----------------|------|----------------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. |
| TCAS | CAS* Pulse Width | 1 | - | 20 | - | 16.7 | - |
| TCRP | CAS* to RAS* Precharge Time | 2 | - | 40 | - | 33.4 | - |
| TCSH | CAS* Hold Time | 4 | - | 80 | - | 66.8 | - |
| TPC | CAS* Cycle Time | 2 | - | 40 | - | 33.4 | - |
| TCP | CAS* Precharge Time | 1 | - | 20 | - | 16.7 | - |
| TRP | RAS* Precharge Time | 3 | - | 60 | - | 50.1 | - |
| TRC | RAS* Cycle Time | 7 | - | 140 | - | 116.9 | - |
| TRAS | RAS* Pulse Width | 4 | - | 80 | - | 66.8 | - |
| TRCD | RAS* to CAS* Delay Time | 3 | - | 60 | - | 50.1 | - |
| TRAH | Row Address Hold Time | 2 | - | 40 | - | 33.4 | - |
| TAR | Column Address Hold From RAS* | 4 | - | 80 | - | 66.8 | - |
| TASC | Column Address Setup Time | 1 | - | 20 | - | 16.7 | - |
| TCAH | Column Address Hold Time | 1 | - | 20 | - | 16.7 | - |
| TWCR | Write Command Hold Referenced to RAS* | 3.5 | - | 70 | - | 58.5 | - |
| TDS | Data-in Setup Time | 0.5 | - | 10 | - | 8.4 | - |
| TDH | Data-in Hold Time | 1 | - | 20 | - | 16.7 | - |
| TDHR | Data Hold Referenced to RAS* | 4 | - | 80 | - | 66.8 | - |
| TASR | Row-Address Setup Time | 0 | - | 0 | - | 0 | - |
| TOE | Output Enable Time | - | 20 | - | 20 | - | 20 |
| TCOH | Data Output Hold after CAS* LOW (Only for EDO-DRAM) | - | - | 5 | - | 5 | - |

(Units: ns)

Required Timing Table

| Sym. | Parameter | T-Value | | MCLK 50MHz | | MCLK 60MHz | |
|------|--------------------------------------|---------|------|---------------|------|---------------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. |
| TCPA | Data Access Time from CAS* Precharge | - | 2 | - | 40 | - | 33.3 |
| TRAC | Data Access Time from RAS* | - | 4 | - | 80 | - | 66.6 |
| TCAC | Data Access Time from CAS* | - | 1 | - | 20 | - | 33.3 |
| TCAA | Data Access Time form Column Address | - | 2 | - | 40 | - | 66.6 |

(Units: ns)

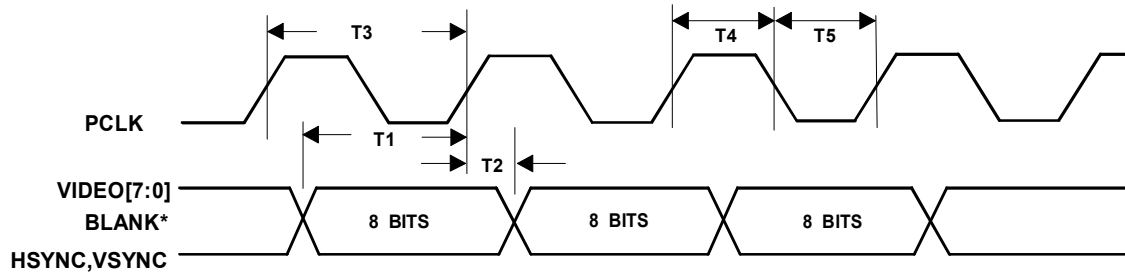


Figure 7.8 Video Timing 4, 8, 24 Bits/Pixel Modes

4,8,16 and 24 BPP Video AC Timing Table

| Symbol | Parameter | Min. | Max. | Notes |
|----------------|-------------------------------------|------|------|-------|
| T ₁ | VIDEO[7:0], BLANK*, SYNC Setup Time | 1.5 | - | |
| T ₂ | VIDEO[7:0], BLANK*, SYNC Hold Time | 1.5 | - | |
| T ₃ | PCLK Period | 7 | - | |
| T ₄ | PCLK High Time | 3 | - | |
| T ₅ | PCLK Low Time | 3 | - | |

(Units: ns)

Shared Memory Arbitration Timing

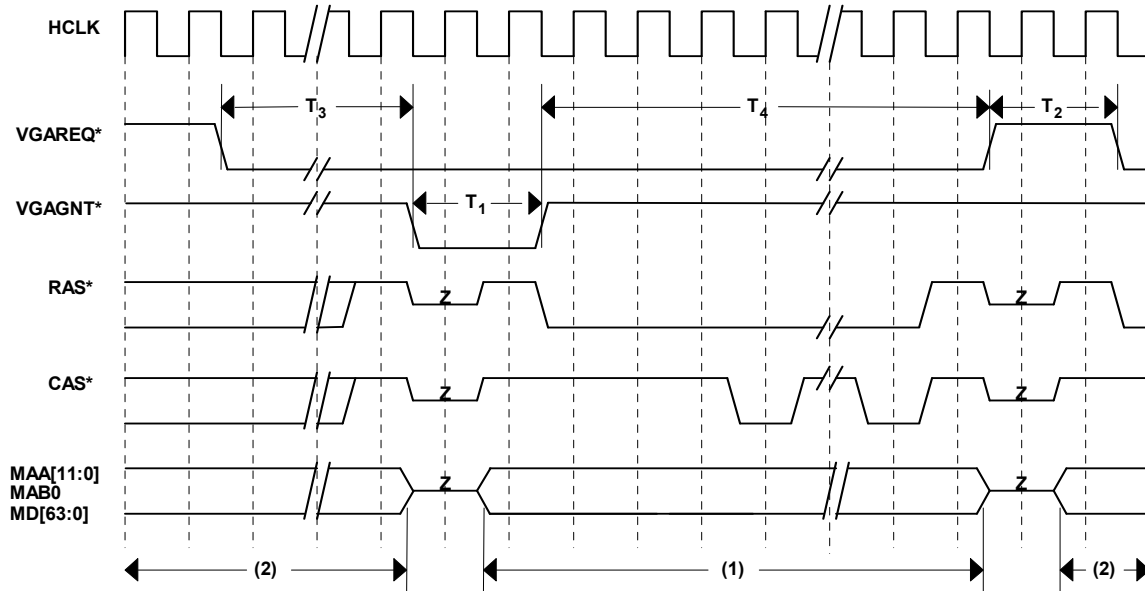


Figure 7.9 Shared Memory Arbitration Timing (I)

- (1) The DRAM is driven by SiS 6205.
- (2) The DRAM is driven by chip set.

T3: When SiS 6205 asserts VGAREQ* to request DRAM bus, the chip-set must assert the VGAGNT* after a period of T3. The maximum period time of T3 is 600 ns.

T1: The chip-set must assert the VGAGNT* at least 2 HCLK cycles.

T4: If the VGAGNT* is deasserted, SiS 6205 will deassert VGAREQ* after a period of T4. The maximum period time of T4 is 1000 ns. SiS 6205 will drive RAS*, CAS*, MA, MD, WE and OE high one HCLK cycle, and then tri-state them.

T2: The SiS 6205 will deassert VGAREQ* at least 2 HCLK cycles.

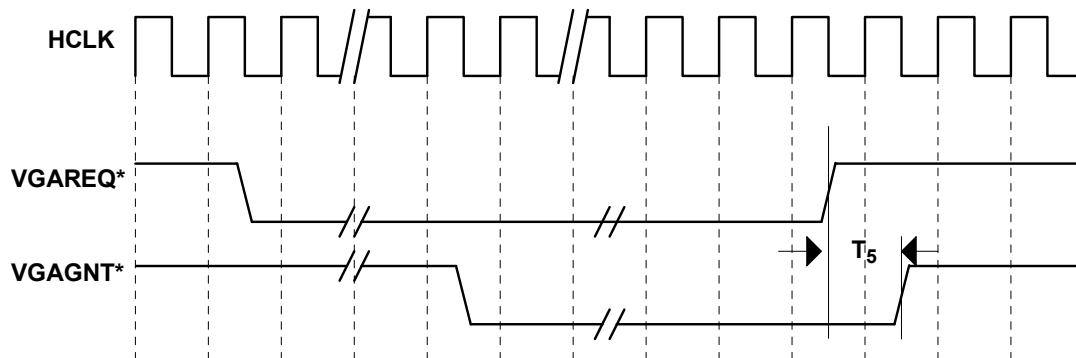


Figure 7.10 Shared Memory Arbitration Timing (II)

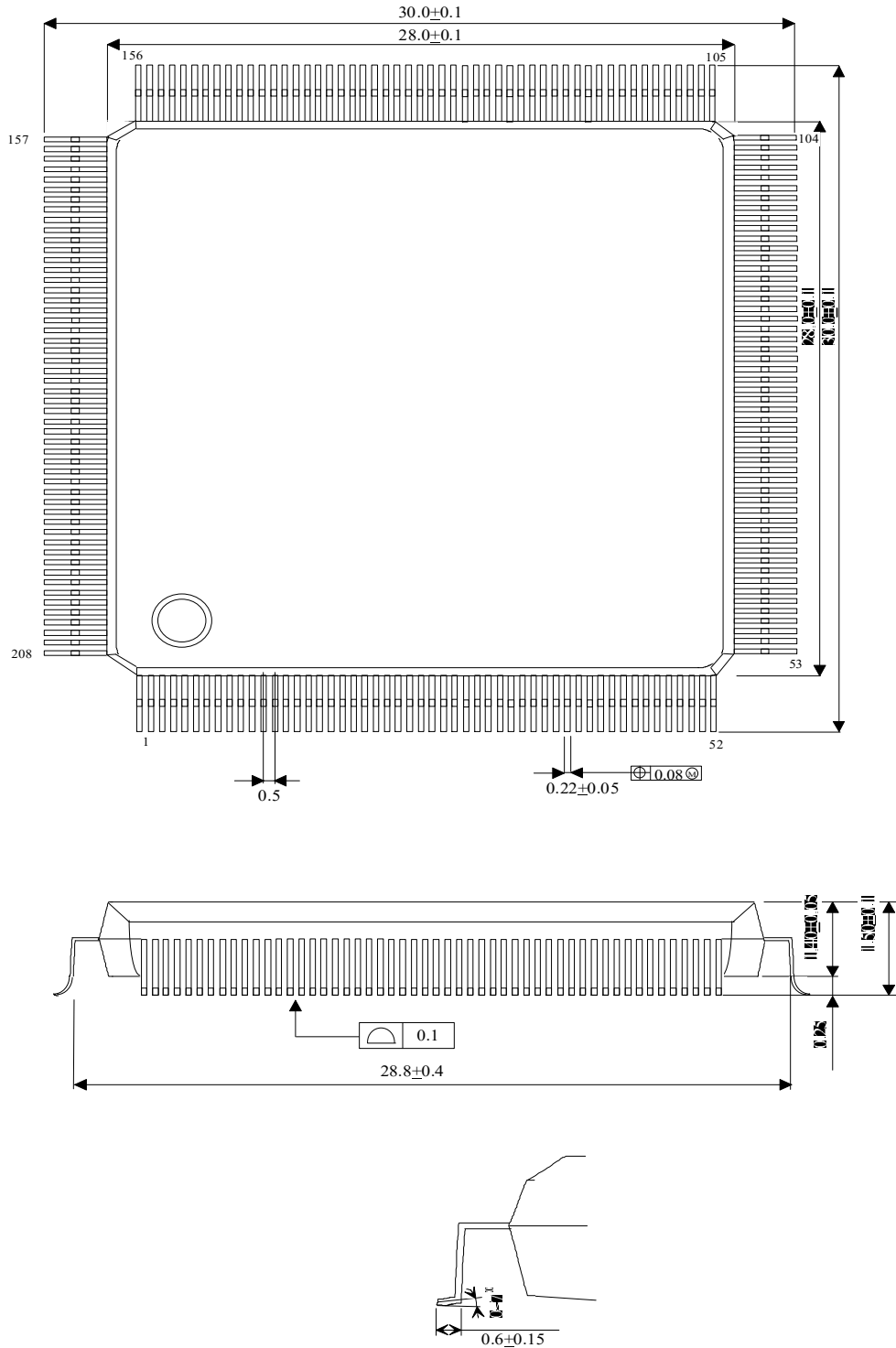
T5: If VGAREQ* is deasserted when VGAGNT* is still asserted, the chip-set should deasserts VGAGNT* after one HCLK cycle.

8. Mechanical Dimension

QFP208-P

(208-Pin Plastic Flat Package)

Unit: mm



**9. Appendix A. Recommended Memory Configuration****1M Byte Display Memory Using 256Kx4 DRAM**

| | U1 | U2 | U3 | U4 |
|-------|----------|----------|----------|-----------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| CAS* | CASA0* | CASA0* | CASA1* | CASA1* |
| WE* | WEA* | WEA* | WEA* | WEA* |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:3] | MD[4:7] | MD[8:11] | MD[12:15] |
| PLANE | 0 | 0 | 1 | 1 |
| Bank | 0 | 0 | 0 | 0 |

| | U5 | U6 | U7 | U8 |
|-------|-----------|-----------|-----------|-----------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| CAS* | CASA2* | CASA2* | CASA3* | CASA3* |
| WE* | WEA* | WEA* | WEA* | WEA* |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] | MAA[0:8] | MAA[0:8] |
| DATA | MD[16:19] | MD[20:23] | MD[24:27] | MD[28:31] |
| PLANE | 2 | 2 | 3 | 3 |
| Bank | 0 | 0 | 0 | 0 |

1M Byte Display Memory Using 2-CAS 256Kx16 DRAM

| | U1 | U2 |
|-------|----------|-----------|
| RAS* | RAS0* | RAS0* |
| CASU* | CASA1* | CASA3* |
| CASL* | CASA0* | CASA2* |
| WE* | WEA* | WEA* |
| OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:15] | MD[16:31] |
| PLANE | 0,1 | 2,3 |
| Bank | 0 | 0 |

**1M Byte Display Memory Using 2-WE 256Kx16 DRAM**

| | U1 | U2 |
|-------|--------------|--------------|
| RAS* | RAS0* | RAS0* |
| WEU* | CASA1* (# a) | CASA3* (# a) |
| WEL* | CASA0* (# a) | CASA2* (# a) |
| CAS* | WEA* (# b) | WEA* (# b) |
| OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:15] | MD[16:31] |
| PLANE | 0,1 | 2,3 |
| Bank | 0 | 0 |

a : CASA*[0:3] pin becomes WEA*[0:3] for dual-WE 256K x 16 Dynamic RAM.

b : WEA* pin becomes CASA* pin for dual-WE 256K x 16 Dynamic RAM.

2M Byte Display Memory Using 2-CAS 256Kx16 DRAM

| | U1 | U2 | U3 | U4 |
|-------|----------|-----------|-----------|-----------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| CASU* | CASA1* | CASA3* | CASA5* | CASA7* |
| CASL* | CASA0* | CASA2* | CASA4* | CASA6* |
| WE* | WEA* | WEA* | WEA* | WEA* |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:15] | MD[16:31] | MD[32:47] | MD[48:63] |
| PLANE | 0,1 | 2,3 | 0,1 | 2,3 |
| Bank | 0 | 0 | 1 | 1 |

2M Byte Display Memory Using 2-WE 256Kx16 DRAM

| | U1 | U2 | U3 | U4 |
|-------|--------------|--------------|--------------|--------------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| WEU* | CASA1* (# a) | CASA3* (# a) | CASA5* (# a) | CASA7* (# a) |
| WEL* | CASA0* (# a) | CASA2* (# a) | CASA4* (# a) | CASA6* (# a) |
| CAS* | WEA* (# c) | WEA* (# c) | WEA* (# c) | WEA* (# c) |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:15] | MD[16:31] | MD[32:47] | MD[48:63] |
| PLANE | 0,1 | 2,3 | 0,1 | 2,3 |
| Bank | 0 | 0 | 1 | 1 |

a : CASA*[0:7] pin becomes WEA*[0:7] for dual-WE 256K x 16 Dynamic RAM.

b : CASB*[0:7] pin becomes WEB*[0:7] for dual-WE 256K x 16 Dynamic RAM.

c : WEA* pin becomes CASA* pin for dual-WE 256K x 16 Dynamic RAM.

d : WEB* pin becomes CASB* pin for deal-WE 256K x 16 Dynamic RAM.

**4M Byte Display Memory Using 2-CAS 256Kx16 DRAM**

| | U1 | U2 | U3 | U4 |
|-------|----------|-----------|-----------|-----------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| CASU* | CASA1* | CASA3* | CASA5* | CASA7* |
| CASL* | CASA0* | CASA2* | CASA4* | CASA6* |
| WE* | WEA* | WEA* | WEA* | WEA* |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:15] | MD[16:31] | MD[32:47] | MD[48:63] |
| PLANE | 0,1 | 2,3 | 0,1 | 2,3 |
| Bank | 0 | 0 | 1 | 1 |

| | U5 | U6 | U7 | U8 |
|-------|------------------|------------------|------------------|------------------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| CASU* | CASB1* | CASB3* | CASB5* | CASB7* |
| CASL* | CASB0* | CASB2* | CASB4* | CASB6* |
| WE* | WEB* | WEB* | WEB* | WEB* |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAB0 MAA[1:8] | MAB0 MAA[1:8] | MAB0 MAA[1:8] | MAB0 MAA[1:8] |
| DATA | MD[0:15] | MD[16:31] | MD[32:47] | MD[48:63] |
| PLANE | 0,1 | 2,3 | 0,1 | 2,3 |
| Bank | 2 | 2 | 3 | 3 |

**4M Byte Display Memory Using 2-WE 256Kx16 DRAM**

| | U1 | U2 | U3 | U4 |
|-------|--------------|--------------|--------------|--------------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| WEU* | CASA1* (# a) | CASA3* (# a) | CASA5* (# a) | CASA7* (# a) |
| WEL* | CASA0* (# a) | CASA2* (# a) | CASA4* (# a) | CASA6* (# a) |
| CAS* | WEA* (# c) | WEA* (# c) | WEA* (# c) | WEA* (# c) |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAA[0:8] | MAA[0:8] | MAA[0:8] | MAA[0:8] |
| DATA | MD[0:15] | MD[16:31] | MD[32:47] | MD[48:63] |
| PLANE | 0,1 | 2,3 | 0,1 | 2,3 |
| Bank | 0 | 0 | 1 | 1 |

| | U5 | U6 | U7 | U8 |
|-------|------------------|------------------|------------------|------------------|
| RAS* | RAS0* | RAS0* | RAS0* | RAS0* |
| WEU* | CASB1* (# b) | CASB3* (# b) | CASB5* (# b) | CASB7* (# b) |
| WEL* | CASB0* (# b) | CASB2* (# b) | CASB4* (# b) | CASB6* (# b) |
| CAS* | WEB* (# d) | WEB* (# d) | WEB* (# d) | WEB* (# d) |
| OE* | OE* | OE* | OE* | OE* |
| ADDR | MAB0 MAA[1:7] | MAB0 MAA[1:7] | MAB0 MAA[1:7] | MAB0 MAA[1:7] |
| DATA | MD[0:15] | MD[16:31] | MD[32:47] | MD[48:63] |
| PLANE | 0,1 | 2,3 | 0,1 | 2,3 |
| Bank | 2 | 2 | 3 | 3 |

a : CASA*[0:3] pin becomes WEA*[0:3] for dual-WE 256K x 16 Dynamic RAM.

b : CASB*[0:3] pin becomes WEB*[0:3] for dual-WE 256K x 16 Dynamic RAM.

c : WEA* pin becomes CASA* pin for dual-WE 256K x 16 Dynamic RAM.

d : WEB* pin becomes CASB* pin for dual-WE 256K x 16 Dynamic RAM.



10. Appendix B. Product Change Notice For Rev. Dx

Major Spec Improved or Modified in Rev. Dx

Performance

- Built-in Direct Draw Accelerator
- Built-in 64x32 CRT FIFOs to support super high resolution graphics modes and reduce CPU wait-state

Integration

- Built-in Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) video decoder interface
- Partially supports VMI (Video Module Interface) to connect to VMI device
- Built-in standard feature connector logic support

Display Memory Interface

- 64-bit display memory data bus architecture with up to 240 MByte/sec peak memory bandwidth by using 2 banks or 4 banks of DRAM.
- Supports 1MB, 2MB, and 4MB DRAM configuration
- Supports 0.5MB, 1MB, 1.5MB, 2MB 2.5MB, 3MB, 3.5MB and 4MB DRAM configuration at shared-memory architecture

Resolution, Color & Frame Rate

- Supports 85Hz vertical refresh rate

Video Functions

- Built-in Philips SAA7110 / SAA7111 and Brooktree Bt815/817/819A (8-bit SPI mode 1, 2) video decoder interface
- Partially supports VMI (Video Module Interface) interface to connect to other VMI devices
- Built-in standard feature connector logic support
- Supports graphics/video overlay function by color-key and/or chroma-key operation
- Supports multi-format Video For Windows such as YUV422, RGB565, and RGB555
- Supports horizontal 2-tap, 8-phase DDA interpolation
- Supports vertical 2-tap, 8-phase DDA interpolation for better quality of video windows expansion
- Built-in 64x16 video capture FIFOs to support video capture
- Built-in two 64x90 video playback line buffers to support video playback
- Supports color key and chroma key overlay
- Supports 3-bit blending
- Supports DCI Drivers
- Supports Direct Draw Drivers

Power Management

- Built-in a low power signal pin for supporting external power down controller

**Pin Definition Changed**

| Pin No. | Pin Name in Rev. Dx | Pin Name in Previous Rev. | Impact |
|----------------|--------------------------------|--------------------------------------|--|
| 63 | PWDN* | OEB* | No impact on old design since this pin is not used in old design. |
| 112 | OE* | OEA* | No impact on old design since it is just changed a name. |
| 159 | UVOE* mux with VMICS* | UVOE* | No impact on old design since it is controlled by MD28 and is default as old design. |
| 160 | YOE* mux with VACTIVE | YOE* | No impact on old design since it is controlled by MD28 and is default as old design. |
| 162 | LLC1 mux with INTREQ | LLC1 | No impact on old design since it is controlled by MD28 and is default as old design. |



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